Allwinner H5 Datasheet

Quad-Core OTT Box Processor

Revision 1.0

May.20,2016

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Revision History

Revision	Date	Description
1.0	May. 20,2016	Initial Release Version

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Chapter 1 About This Documentation

1.1. Purpose

This documentation provides an overall description of the Allwinner's H5 application processor, which describes the overview, features, logical structures ,functions and register listings of each module. The documentation also describes pin/signal characteristics, operating modes, current consumption, the interface timing and package. The documentation is intended to be used by board-level product designers and product hardware/software developers. This documentation assumes that the reader has a background in computer engineering and/or hardware designing and/or software engineering.

1.2. Acronyms and Abbreviations

The table below contains acronyms and abbreviations used in this documentation.

AES	Advanced Encryption Standard
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AHB	AMBA High-speed Bus
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
CIR	Consumer Infrared
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression

DSI	MIPI Display Serial Interface
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FIFO	First In First Out
GIC	Generic Interrupt Controller
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
KEYADC	Analog to Digital Converter for Key
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MII	Media Independent Interface
MIPI	Mobile Industry Processor Interface
MIPI DSI	MIPI Display Serial Interface
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MPEG1	The First MPEG Compression Scheme Specification
MPEG4	The Most Current MPEG Compression Scheme Specification
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
OHCI	Open Host Controller Interface
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
R	Read only/non-Write

RGB	Read Green Blue
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RTC	Real Time Clock
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete.Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has non-effect
R/W1C	Read/Write 1 to Clear, Writing 0 has non-effect
R/W1S	Read/Write 1 to Set, Writing 0 has non-effect
SDIO	Secure Digital Input Output
SDRAM	Sychronous Dynamic Random Access Memory
SOC	System On Chip
SPI	Serial Peripheral Interface
S/PDIF	Sony/Philips Digital Interface Format
SRAM	Static Random Access Memory
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

Chapter 2 Overview

This part describes the overview for H5 processor.

2.1. Processor Overview

The Allwinner H5 is a highly cost-efficient quad-core OTT Box processor, which is a part of growing home entertainment products that offer high-performance processing with a high degree of functional integration.

The H5 processor has some very exciting features, for example:

- **CPU**: Quad-core ARM Cortex™-A53 Processor, a power-efficient ARM v8 architecture, it has 64 and 32bit execution states for scalable high performance ,which includes a NEON multimedia processing engine.
- **Graphics**: The hexa-core ARM Mali450 GPU including dual Geometry Processors(GP) and quad Pixel Processors(PP), provides users with superior experience in video playback and mainstream game; OpenGL ES2.0 and OpenVG1.1 standards are supported.
- **Video Engine**: H5 provides multi-format high-definition video encoder/decoder with dedicated hardware, including H.265 decoder by 4K@30fps , H.264 decoder by 4K@30fps, MPEG1/2/4 decoder by 1080p@60fps, VP8/AVS jizhun decoder by 1080p@60fps, VC1 decoder by 1080p@30fps, H.264 encoder by 1080p@60fps.
- **Display Subsystem**: Supports DE2.0 for excellent display experience, and two display interfaces for HDMI1.4 and CVBS display.
- **Memory Controller**: The processor supports many types of external memory devices, including DDR3/DDR3L, NAND Flash(MLC,SLC,TLC,EF),Nor Flash, SD/SDIO/MMC including eMMC up to rev5.1.
- **Security System**: The processor delivers hardware security features that enable trustzone security system, Digital Rights Management(DRM) , information encryption/decryption, secure boot, secure JTAG and secure efuse.
- **Interfaces**: The processor has a broad range of hardware interfaces such as parallel CMOS sensor interface, 10/100/1000Mbps EMAC with FE PHY, USB OTG v2.0 operating at high speed(480Mbps) with PHY, USB Host with PHY and a variety of other popular interfaces(SPI,UART,CIR,TSC,TWI,SCR).

2.2. Processor Features

2.2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 MPCore™ Processor
- Thumb-2 Technology
- Supports NEON Advanced SIMD(Single Instruction Multiple Data)instruction for acceleration of media and signal processing functions
- Supports Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- Independent 32KB L1 Instruction cache and 32KB L1 Data cache
- Shared 512KB L2-cache

2.2.2. GPU Architecture

- Hexa-core ARM Mali450 GPU
- Dual Geometry Processors with 32KB L2 cache
- Quad Pixel Processors with 128KB L2 cache
- Concurrent multi-core processing
- 3000Mpix/sec and 163Mtri/sec
- Full scene over-sampled 4X anti-aliasing engine with no additional bandwidth usage
- OpenGL ES 1.1/2.0 and OpenVG 1.1 support

2.2.3. Memory Subsystem

2.2.3.1. Boot ROM

- On chip ROM
- Supports secure and non-secure access boot
- Supports system boot from the following devices:
  - NAND Flash
  - SD/TF card
  - eMMC
  - Nor Flash
- Supports system code download through USB OTG

2.2.3.2. SDRAM

- Compatible with JEDEC standard DDR3/DDR3L SDRAM
- Supports clock frequency up to 667MHz(DDR3-1333)
- 32-bit bus width
- Up to 3GB address space
- Supports 2 chip selects
- 16 address signal lines and 3 bank signal lines
- Supports Memory Dynamic Frequency Scale(MDFS)
- Random read or write operation is supported

2.2.3.3. NAND Flash

- Compliant with ONFI 2.3 and Toggle 1.0
- Up to 2 flash chips
- 8-bit data bus width
- Up to 64-bit ECC per 1024 bytes
- Supports 1024, 2048, 4096, 8192, 16K bytes size per page
- Supports SLC/MLC/TLC flash and EF-NAND memory
- Supports SDR, ONFI DDR and Toggle DDR NAND
- Embedded DMA to do data transfer
- Supports data transfer together with normal DMA

2.2.3.4. SMHC

- Up to 3 SD/MMC host controller(SMHC) interfaces
- Complies with eMMC standard specification V5.1, SD physical layer specification V3.0, SDIO card specification V3.0
- 1-bit or 4-bit data bus transfer mode for SD/TF cards up to 50MHz in SDR mode
- 1-bit or 4-bit data bus transfer mode for connecting to an external Wi-Fi module up to 150MHz in SDR mode and 50MHz in DDR mode
- 1-bit ,4-bit or 8-bit data bus transfer mode for MMC cards up to 150MHz in SDR mode or 100MHz in DDR mode
- Supports block size of 1 to 65535 bytes
- Embedded special DMA to do data transfer
- Supports hardware CRC generation and error detection

2.2.4. System Peripheral

2.2.4.1. Timer

- 2 on-chip Timers with interrupt-based operation
- 1 watchdog to generate reset signal or interrupt
- Two 33-bit Audio/Video Sync(AVS) Counter to synchronize video and audio in the player

2.2.4.2. High Speed Timer

- 1 High Speed Timer with 56-bit counter
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register
- Clock source is synchronized with AHB clock, much more accurate than other timers

2.2.4.3. RTC

- Time,calendar
- Counters second,minutes,hours,day,week,month and year with leap year generator
- Alarm:general alarm and weekly alarm
- One 32KHz fanout

2.2.4.4. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 125 Shared Peripheral Interrupts(SPIs)

2.2.4.5. DMA

- Up to 12-channel DMA
- Interrupt generated for each DMA channel
- Transfers data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Programs the DMA burst size
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

2.2.4.6. CCU

- 9 PLLs
- Supports an external 24MHz crystal oscillator and an on-chip 16MHz RC oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.2.4.7. PWM

- Supports outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency

2.2.4.8. Thermal Sensor

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- 2 temperature-sensing cell embedded :sensor0 for CPU,sensor1 for GPU

2.2.4.9. KEYADC

- Analog to digital converter with 6-bit resolution for key application
- Maximum sampling frequency up to 250 Hz
- Supports general key, hold key and already hold key
- Supports single , normal and continuous work mode

2.2.4.10. Message Box

- Two users for Message Box instance
- Eight Message Queues for the MSGBox instance
- Each of Queues could be configured as transmitter or receiver for user
- Two interrupts for the MSGBox instance
- Register polling for the MSGBox instance
- 32-bit message width
- Four-message FIFO depth for each message queue

2.2.4.11. Spinlock

- 32 spinlocks
- Two kinds of status of lock register: TAKEN and NOT TAKEN

2.2.4.12. Crypto Engine(CE)

- Supports symmetrical algorithm: AES, DES, TDES
- Supports hash algorithm:SHA-1/SHA-224/SHA-256,MD5,HMAC
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit TRNG
- Supports ECB,CBC, CTR, CTS modes for AES
- Supports ECB, CBC, CTR modes for DES
- Supports ECB, CBC, CTR modes for TDES
- 128-bit, 192-bit and 256-bit key size for AES
- Embedded special DMA to do data transfer

2.2.4.13. Security ID(SID)

- Supports 2K-bit EFUSE for chip ID and security application

2.2.4.14. CPU Configuration

- Configure related CPU parameters, including power on, reset, cache, debug, and check the status of CPU
- One 64-bit common counter

2.2.5. Display Subsystem

2.2.5.1. DE2.0

- Output size up to 4096x4096
- Supports four alpha blending channel for main display, two channel for aux display
- Supports four overlay layers in each channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor 2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports writeback for high efficient dual display

2.2.5.2. Display Output

- Supports HDMI V1.4 output up to 4K@30fps
  - Compatible with HDMI 1.4 specification
  - Compatible with HDCP 1.2 for HDMI
  - Supports EDID block read by DDC
  - Supports HPD
  - Integrated CEC hardware
  - Supports TMDS clock from 27MHz to 297MHz
  - Supports RGB888,YUV444 video formats with only 8bit color depth
    4K@30Hz
    1920 x 1080p@50/60Hz
    1920 x 1080p@24Hz
    1920 x 1080i@50/60Hz

1280 x 720p@50/60Hz
720 x 480p@60Hz
720 x 576p@50Hz
3D Frame Packing 1920 x 1080p@24Hz

- Supports L-PCM audio format
  Up to 192KHz IEC-60958 audio sampling rate
  Maximum 24bit, 8 channel
- Supports IEC-61937 compressed audio format

- Supports TV CVBS output
  - Standard NTSC-M and PAL-B,D,G,H,I output
  - Plug status auto detecting

2.2.6. Video Engine

2.2.6.1. Video Decoder

- Supports multi-format video playback, including:
  - H.265 MP/L5.0: 4K@30fps
  - H.264 BP/MP/HP Level4.2: 4K@30fps
  - H.263 BP: 1080p@60fps
  - MPEG1 MP/HL: 1080p@60fps
  - MPEG2 MP/HL: 1080p@60fps
  - MPEG4 SP/ASP L5: 1080p@60fps
  - Sorenson Spark: 1080p@60fps
  - VP8 N/A: 1080p@60fps
  - VC1 SP/MP/AP: 1080p@30fps
  - AVS/AVS+ jizhun: 1080p@60fps
  - xvid N/A: 1080p@60fps
  - MJPEG: 1080p@30fps
- Supports 1080p blu-ray 3D
- Supports 3D size:3840x1080,1920x2160
- Supports decoding output format:YV12

2.2.6.2. Video Encoder

- Supports H.264 video encoder up to 1080p@60fps
- Supports input picture size up to 4800x4800
- Supports input format: tiled (128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Supports Alpha blending
- Supports thumb generation
- Supports 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Supports rotated input

2.2.7. Image Subsystem

2.2.7.1. CSI

- Supports 8-bit YUV422 CMOS sensor interface
- Supports CCIR656 protocol for NTSC and PAL
- Up to 5M pixel camera sensor
- Supports video capture resolution up to 1080p@30fps

2.2.8. Audio Subsystem

2.2.8.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
  - 100 ± 3 dB SNR@A-weight
  - Supports ADC sample rate from 8 KHz to 192 KHz
- Two audio analog-to-digital(ADC) channels
  - 93 ± 3 dB SNR@A-weight
  - Supports ADC sample rate from 8 KHz to 48 KHz
- Supports analog/ digital volume control
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- Supports Dynamic Range Control(DRC) adjusting the ADC recording input
- Three audio inputs:
  - Two differential microphone inputs
  - One stereo Line-in L/R channel input
- One audio output: Stereo line-out L/R channel output

2.2.8.2. I2S/PCM

- 2 I2S/PCM controllers
- Compliant with standard Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Supports 8-channel in TDM mode
- Full-duplex synchronous work mode
- Mater and slave mode configured
- Clock up to 100 MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 KHz to 192 KHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- Supports programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Programmable FIFO thresholds

2.2.8.3. One Wire Audio(OWA)

- IEC-60958 transmitter functionality
- Compliance with S/PDIF Interface
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 32×24 bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds

2.2.9. External Peripherals

2.2.9.1. USB

- One USB 2.0 OTG,with integrated USB PHY
  - Complies with USB2.0 Specification
  - Supports High-Speed (HS,480Mbps),Full-Speed(FS,12Mbps) and Low-Speed(LS,1.5Mbps) in host mode
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 8 User-Configurable Endpoints in device mode
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- Three USB Host, with integrated USB PHY
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.

2.2.9.2. Ethernet

- Integrated an internal 10/100M PHY
- Supports 10/100/1000Mbps data transfer rate
- Supports MII/RGMII/RMII interface
- Supports full-duplex and half-duplex operation
- Programmable frame length
- Automatic CRC and pad generation controllable on a per-frame basis
- Options for Automatic Pad/CRC Stripping on receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Programmable Inter Frame Gap (40-96 bit times in steps of 8)
- Supports a variety of flexible address filtering modes

2.2.9.3. CIR

- A flexible receiver for IR remote

- Programmable FIFO threshold

2.2.9.4. UART

- Up to 5 UART controllers, one UART for CPUx debug, one UART for CPUs debug, others for UART applications
- UART0: 2-wire; UART1/2/3: 4-wire; S_UART: 2-wire
- Compliant with industry-standard 16450 and 16550 UARTs
- Supports word length from 5 to 8 bits, an optional parity bit and 1,1.5 or 2 stop bits
- Programmable parity(even, odd and no parity)
- 64-byte Transmit and receive data FIFOs for all UART

2.2.9.5. SPI

- Up to 2 SPI controllers
- Full-duplex synchronous serial interface
- Master/Slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64-byte FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation supported
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable
- The maximum frequency is 100MHz
- Supports single and dual read mode

2.2.9.6. TWI

- Up to 4 TWI(Two Wire Interface) controllers
- Supports Standard mode(up to 100K bps) and Fast mode(up to 400K bps)
- Master/Slave configurable
- Allows 10-bit addressing transactions
- Perform arbitration and clock synchronization
- Allows operation from a wide range of input clock frequencies

2.2.9.7. TSC

- Up to 4 TSC(Transport Stream Controller)
- Compliant with the industry-standard AMBA Host Bus(AHB) Specification, Revision 2.0.Supports 32-bit Little Endian bus
- Supports DVB-CSA V1.1 Descrambler
- One external Synchronous Parallel Interface(SPI) or one external Synchronous Serial Interface(SSI)
- Configurable SPI and SSI timing parameters
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting

2.2.9.8. SCR

- Up to 2 SCR(Smart Card Reader) controllers
- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card

2.2.10. Package

- FBGA 347 balls, 0.65mm ball pitch, 14mm x 14mm

2.3. System Block Diagram

Figure 2-1 shows the block diagram of H5 processor.

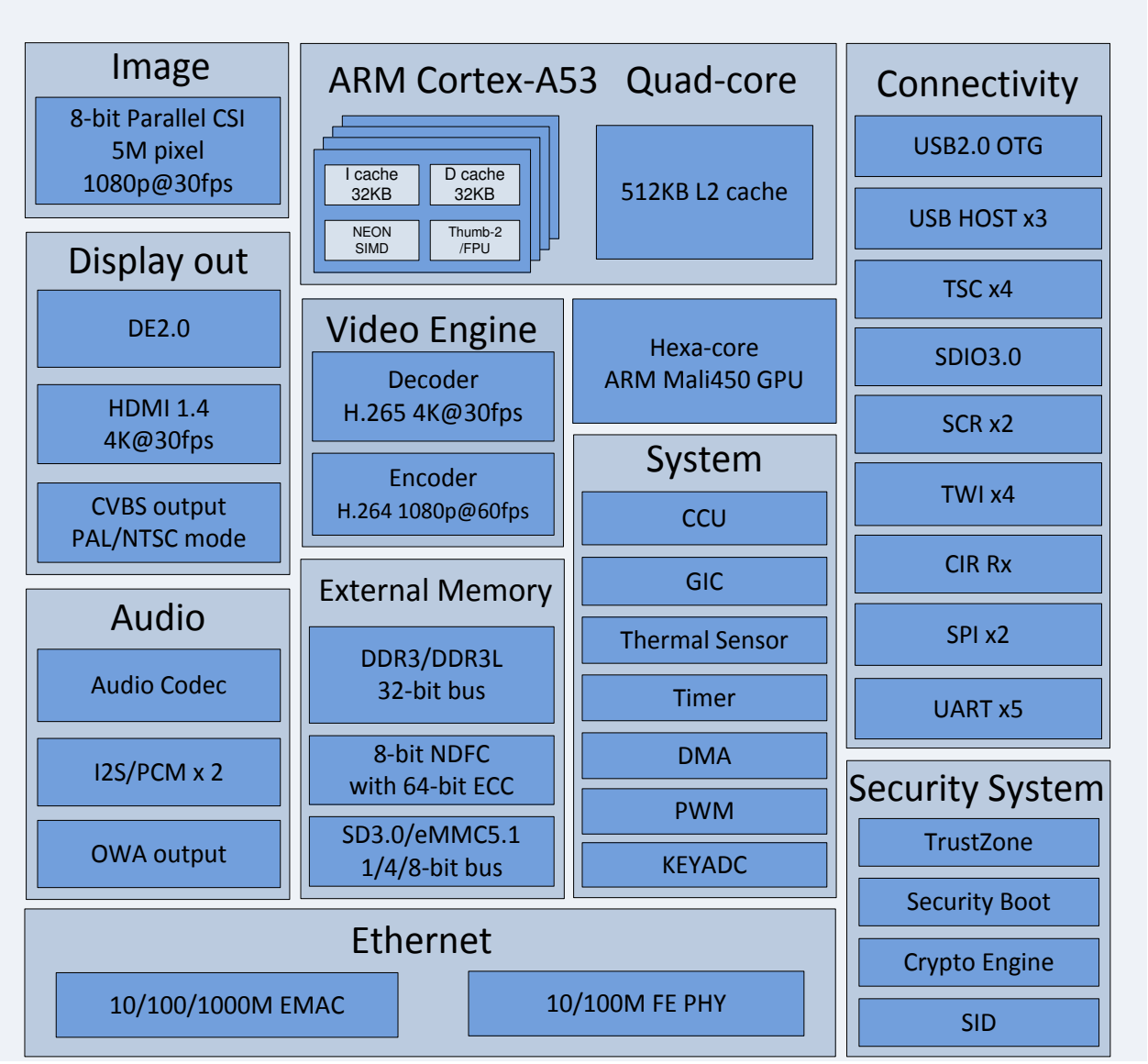


Figure 2-1. H5 Block Diagram

Chapter 3 Pin Description

This part details the H5 pin description from the following aspects:

- Pin Characteristics
- Signal Descriptions

3.1. Pin Characteristics

Table 3-1 lists the characteristics of H5 Pins from seven aspects: BALL#, Pin Name, Default Function, Type, Reset State, Default Pull Up/Down, and Buffer Strength.

(1).**Ball#** : Package ball numbers associated with each signals.
(2).**Pin Name** : The name of the package pin.
(3).**Signal Name** : The signal name for that pin in the mode being used.
(4).**Function** : Multiplexing function number.
(5).**Ball Reset Rel. Function** : The function is automatically configured after RESET from low to high.
(6).**Type** : Denotes the signal direction
I (Input),
O (Output),
I/O(Input / Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)
(7).**Ball Reset State** : The state of the terminal at reset.
Z(High-impedance)
(8).**Pull Up/Down** : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up(PU) and Pull-down(PD) resistors can be enabled or disabled via software.
(9).**Buffer Strength** : Defines drive strength of the associated output buffer.
(10).**Power Supply** : The voltage supply for the terminal's IO buffers.

Table 3-1. Pin Characteristics

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
DRAM									
T17	SA0	SA0	NA	NA	O	Z	NA	NA	VCC-DRAM
U18	SA1	SA1	NA	NA	O	Z	NA	NA	VCC-DRAM
V19	SA2	SA2	NA	NA	O	Z	NA	NA	VCC-DRAM
V20	SA3	SA3	NA	NA	O	Z	NA	NA	VCC-DRAM
V21	SA4	SA4	NA	NA	O	Z	NA	NA	VCC-DRAM
Y19	SA5	SA5	NA	NA	O	Z	NA	NA	VCC-DRAM
Y20	SA6	SA6	NA	NA	O	Z	NA	NA	VCC-DRAM
V15	SA7	SA7	NA	NA	O	Z	NA	NA	VCC-DRAM
W18	SA8	SA8	NA	NA	O	Z	NA	NA	VCC-DRAM
Y18	SA9	SA9	NA	NA	O	Z	NA	NA	VCC-DRAM
P19	SA10	SA10	NA	NA	O	Z	NA	NA	VCC-DRAM
N19	SA11	SA11	NA	NA	O	Z	NA	NA	VCC-DRAM
R18	SA12	SA12	NA	NA	O	Z	NA	NA	VCC-DRAM
V12	SA13	SA13	NA	NA	O	Z	NA	NA	VCC-DRAM
N17	SA14	SA14	NA	NA	O	Z	NA	NA	VCC-DRAM
R17	SA15	SA15	NA	NA	O	Z	NA	NA	VCC-DRAM
W17	SBA0	SBA0	NA	NA	O	Z	NA	NA	VCC-DRAM
T18	SBA1	SBA1	NA	NA	O	Z	NA	NA	VCC-DRAM
V17	SBA2	SBA2	NA	NA	O	Z	NA	NA	VCC-DRAM
U15	SCAS	SCAS	NA	NA	O	Z	NA	NA	VCC-DRAM
AA19	SCK	SCK	NA	NA	O	Z	NA	NA	VCC-DRAM
AA20	SCKB	SCKB	NA	NA	O	Z	NA	NA	VCC-DRAM
AA21	SCKE0	SCKE0	NA	NA	O	Z	NA	NA	VCC-DRAM
Y21	SCKE1	SCKE1	NA	NA	O	Z	NA	NA	VCC-DRAM
W20	SCS0	SCS0	NA	NA	O	Z	NA	NA	VCC-DRAM
W21	SCS1	SCS1	NA	NA	O	Z	NA	NA	VCC-DRAM
W11	SODT0	SODT0	NA	NA	O	Z	NA	NA	VCC-DRAM
V11	SODT1	SODT1	NA	NA	O	Z	NA	NA	VCC-DRAM
N20	SDQ0	SDQ0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
P21	SDQ1	SDQ1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
P20	SDQ2	SDQ2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
U21	SDQ3	SDQ3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
R19	SDQ4	SDQ4	NA	NA	I/O	Z	NA	NA	VCC-DRAM
T20	SDQ5	SDQ5	NA	NA	I/O	Z	NA	NA	VCC-DRAM
U19	SDQ6	SDQ6	NA	NA	I/O	Z	NA	NA	VCC-DRAM
U20	SDQ7	SDQ7	NA	NA	I/O	Z	NA	NA	VCC-DRAM
J19	SDQ8	SDQ8	NA	NA	I/O	Z	NA	NA	VCC-DRAM
H20	SDQ9	SDQ9	NA	NA	I/O	Z	NA	NA	VCC-DRAM
H21	SDQ10	SDQ10	NA	NA	I/O	Z	NA	NA	VCC-DRAM
J21	SDQ11	SDQ11	NA	NA	I/O	Z	NA	NA	VCC-DRAM
L20	SDQ12	SDQ12	NA	NA	I/O	Z	NA	NA	VCC-DRAM
L21	SDQ13	SDQ13	NA	NA	I/O	Z	NA	NA	VCC-DRAM
M21	SDQ14	SDQ14	NA	NA	I/O	Z	NA	NA	VCC-DRAM
M19	SDQ15	SDQ15	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y17	SDQ16	SDQ16	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA17	SDQ17	SDQ17	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y16	SDQ18	SDQ18	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W15	SDQ19	SDQ19	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y14	SDQ20	SDQ20	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA14	SDQ21	SDQ21	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y13	SDQ22	SDQ22	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y12	SDQ23	SDQ23	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W12	SDQ24	SDQ24	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA11	SDQ25	SDQ25	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y11	SDQ26	SDQ26	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y10	SDQ27	SDQ27	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W9	SDQ28	SDQ28	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA8	SDQ29	SDQ29	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y8	SDQ30	SDQ30	NA	NA	I/O	Z	NA	NA	VCC-DRAM

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
Y7	SDQ31	SDQ31	NA	NA	I/O	Z	NA	NA	VCC-DRAM
M20	SDQM0	SDQM0	NA	NA	O	Z	NA	NA	VCC-DRAM
G20	SDQM1	SDQM1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA18	SDQM2	SDQM2	NA	NA	O	Z	NA	NA	VCC-DRAM
AA12	SDQM3	SDQM3	NA	NA	O	Z	NA	NA	VCC-DRAM
R20	SDQS0	SDQS0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
R21	SDQS0B	SDQS0B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
K20	SDQS1	SDQS1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
J20	SDQS1B	SDQS1B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA15	SDQS2	SDQS2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y15	SDQS2B	SDQS2B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA9	SDQS3	SDQS3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y9	SDQS3B	SDQS3B	NA	NA	I/O	Z	NA	NA	VCC-DRAM
V13	SRAS	SRAS	NA	NA	O	Z	NA	NA	VCC-DRAM
U16	SRST	SRST	NA	NA	O	Z	NA	NA	VCC-DRAM
T16	SVREF	SVREF	NA	NA	P	NA	NA	NA	VCC-DRAM
W13	SWE	SWE	NA	NA	O	Z	NA	NA	VCC-DRAM
V10	SZQ	SZQ	NA	NA	AI	Z	NA	NA	VCC-DRAM
L16,M16,N16,P16,P17,R16,T12,T13,T14,T15,U11	VCC-DRAM	VCC-DRAM	NA	NA	P	NA	NA	NA	NA
GPIOA									
D11	PA0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_TX	2		O				
		JTAG_MS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT0	6		I				
		IO Disable	7		OFF				
D5	PA1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_RX	2		I				
		JTAG_CK	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT1	6		I				
		IO Disable	7		OFF				
D6	PA2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_RTS	2		O				
		JTAG_DO	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT2	6		I				
		IO Disable	7		OFF				
E13	PA3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_CTS	2		I				
		JTAG_DI	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT3	6		I				
		IO Disable	7		OFF				
F5	PA4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART0_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT4	6		I				
		IO Disable	7		OFF				
H6	PA5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Output	1		O				
		UART0_RX	2		I				
		PWM0	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT5	6		I				
		IO Disable	7		OFF				
E14	PA6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_PWREN	2		O				
		PCM0_MCLK	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT6	6		I				
		IO Disable	7		OFF				
D8	PA7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT7	6		I				
		IO Disable	7		OFF				
F13	PA8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_DATA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT8	6		I				
		IO Disable	7		OFF				
D13	PA9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_RST	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT9	6		I				
		IO Disable	7		OFF				
E11	PA10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SIM0_DET	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT10	6		I				
		IO Disable	7		OFF				
F11	PA11	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI0_SCK	2		I/O				
		DI_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT11	6		I				
		IO Disable	7		OFF				
C13	PA12	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI0_SDA	2		I/O				
		DI_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT12	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
E15	PA13	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_CS	2		I/O				
		UART3_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT13	6		I				
		IO Disable	7		OFF				
G12	PA14	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_CLK	2		I/O				
		UART3_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT14	6		I				
		IO Disable	7		OFF				
F14	PA15	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_MOSI	2		I/O				
		UART3_RTS	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT15	6		I				
		IO Disable	7		OFF				
D15	PA16	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SPI1_MISO	2		I/O				
		UART3_CTS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT16	6		I				
		IO Disable	7		OFF				
C14	PA17	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		OWA_OUT	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT17	6		I				
		IO Disable	7		OFF				
B13	PA18	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_SYNC	2		I/O				
		TWI1_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT18	6		I				
		IO Disable	7		OFF				
B14	PA19	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_CLK	2		I/O				
		TWI1_SDA	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT19	6		I				
		IO Disable	7		OFF				
A13	PA20	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_DOUT	2		O				
		SIM0_VPPEN	3		O				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		PA_EINT20	6		I				
		IO Disable	7		OFF				
A14	PA21	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		PCM0_DIN	2		I				
		SIM0_VPPPP	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PA_EINT21	6		I				
		IO Disable	7		OFF				
GPIOC									
C15	PC0	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_WE	2		O				
		SPI0_MOSI	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C16	PC1	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_ALE	2		O				
		SPI0_MISO	3		I/O				
		SDC2_DS	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B16	PC2	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CLE	2		O				
		SPI0_CLK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B15	PC3	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE1	2		O				
		SPI0_CS	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
F16	PC4	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE0	2		O				
		Reserved	3		NA				
		SPI0_MISO	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A17	PC5	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RE	2		O				
		SDC2_CLK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E16	PC6	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		NAND_RB0	2		I				
		SDC2_CMD	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A16	PC7	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RB1	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B18	PC8	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ0	2		I/O				
		SDC2_D0	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C17	PC9	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ1	2		I/O				
		SDC2_D1	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
D17	PC10	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ2	2		I/O				
		SDC2_D2	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C18	PC11	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ3	2		I/O				
		SDC2_D3	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B17	PC12	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ4	2		I/O				
		SDC2_D4	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B19	PC13	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ5	2		I/O				
		SDC2_D5	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
F17	PC14	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ6	2		I/O				
		SDC2_D6	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C19	PC15	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ7	2		I/O				
		SDC2_D7	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
H16	PC16	Input	0	Function7	I	PD	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQS	2		O				
		SDC2_RST	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
G15	VCC-PC	VCC-PC	NA	NA	P	NA	NA	NA	NA
GPIOD									
C21	PD0	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD3/ MII_RXD3/ RMII_NULL	2		I				
		DI_TX	3		O				
		TS2_CLK	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
H17	PD1	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD2/ MII_RXD2/ RMII_NULL	2		I				
		DI_RX	3		I				
		TS2_ERR	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B20	PD2	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD1/ MII_RXD1/ RMII_RXD1	2		I				
		Reserved	3		NA				
		TS2_SYNC	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
H18	PD3	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXD0/ MII_RXD0/ RMII_RXD0	2		I				
		Reserved	3		NA				
		TS2_DVLD	4		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A20	PD4	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXCK/ MII_RXCK/ RMII_NULL	2		I				
		Reserved	3		NA				
		TS2_D0	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
F19	PD5	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_RXCTL/ MII_RXDV/ RMII_CRS_DV	2		I				
		Reserved	3		NA				
		TS2_D1	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B21	PD6	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_NULL/ MII_RXERR/ RMII_RXER	2		I				
		Reserved	3		NA				
		TS2_D2	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E18	PD7	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD3/ MII_TXD3/ RMII_NULL	2		O				
		Reserved	3		NA				
		TS2_D3	4		I				
		TS3_CLK	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
E20	PD8	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD2/ MII_TXD2/ RMII_NULL	2		O				
		Reserved	3		NA				
		TS2_D4	4		I				
		TS3_ERR	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
F21	PD9	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD1/ MII_TXD1/ RMII_TXD1	2		O				
		Reserved	3		NA				
		TS2_D5	4		I				
		TS3_SYNC	5		i				
		Reserved	6		NA				
		IO Disable	7		OFF				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
H19	PD10	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXD0/ MII_TXD0/ RMII_TXD0	2		O				
		Reserved	3		NA				
		TS2_D6	4		I				
		TS3_DVLD	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
F20	PD11	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_NULL/ MII_CRS/ RMII_NULL	2		I				
		Reserved	3		NA				
		TS2_D7	4		I				
		TS3_D0	5		I				
		Reserved	6		NA				
		IO Disable	7		OFF				
E19	PD12	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXCK/ MII_TXCK/ RMII_TXCK	2		I/O				
		Reserved	3		NA				
		SIM1_PWREN	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K17	PD13	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_TXCTL/ MII_TXEN/ RMII_TXEN	2		I/O				
		Reserved	3		NA				
		SIM1_CLK	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L17	PD14	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_NULL/ MII_TXERR/ RMII_NULL	2		O				
		Reserved	3		NA				
		SIM1_DATA	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K18	PD15	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		RGMII_CLKIN/ MII_COL/ RMII_NULL	2		I				
		Reserved	3		NA				
		SIM1_RST	4		O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L18	PD16	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		MDC	2		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	3		NA				
		SIM1_DET	4		I				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L19	PD17	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		MDIO	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
J15	VCC-PD	VCC-PD	NA	NA	P	NA	NA	NA	NA
GPIOE									
B10	PE0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_PCLK	2		I				
		TS0_CLK	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A10	PE1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_MCLK	2		O				
		TS0_ERR	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B11	PE2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_HSYNC	2		I				
		TS0_SYNC	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C10	PE3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_VSYNC	2		I				
		TS0_DVLD	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C9	PE4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D0	2		I				
		TS0_D0	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E10	PE5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D1	2		I				
		TS0_D1	3		I				
		Reserved	4		O				
		Reserved	5		NA				
		Reserved	6		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
D10	PE6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D2	2		I				
		TS0_D2	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C8	PE7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D3	2		I				
		TS0_D3	3		I				
		TS1_CLK	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C11	PE8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D4	2		I				
		TS0_D4	3		I				
		TS1_ERR	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C12	PE9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D5	2		I				
		TS0_D5	3		I				
		TS1_SYNC	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
E8	PE10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D6	2		I				
		TS0_D6	3		I				
		TS1_DVLD	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
A11	PE11	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_D7	2		I				
		TS0_D7	3		I				
		TS1_D0	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
B12	PE12	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_SCK	2		I/O				
		TWI2_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C7	PE13	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		CSI_SDA	2		I/O				
		TWI2_SDA	3		I/O				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C6	PE14	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		SIM1_VPPEN	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
C5	PE15	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		SIM1_VPPPP	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
GPIOF									
D19	PF0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D1	2		I/O				
		JTAG_MS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT0	6		I				
		IO Disable	7		OFF				
A19	PF1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D0	2		I/O				
		JTAG_DI	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT1	6		I				
		IO Disable	7		OFF				
D20	PF2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_CLK	2		O				
		UART0_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT2	6		I				
		IO Disable	7		OFF				
F18	PF3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_CMD	2		I/O				
		JTAG_DO	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT3	6		I				
		IO Disable	7		OFF				
E21	PF4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		SDC0_D3	2		I/O				
		UART0_RX	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT4	6		I				
		IO Disable	7		OFF				
C20	PF5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		SDC0_D2	2		I/O				
		JTAG_CK	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT5	6		I				
		IO Disable	7		OFF				
G18	PF6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT6	6		I				
		IO Disable	7		OFF				
GPIOG									
J3	PG0	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT0	6		I				
		IO Disable	7		OFF				
L2	PG1	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CMD	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT1	6		I				
		IO Disable	7		OFF				
H4	PG2	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D0	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT2	6		I				
		IO Disable	7		OFF				
F3	PG3	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D1	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT3	6		I				
		IO Disable	7		OFF				
C2	PG4	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D2	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT4	6		I				
		IO Disable	7		OFF				
C1	PG5	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D3	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT5	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
G4	PG6	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT6	6		I				
		IO Disable	7		OFF				
D3	PG7	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT7	6		I				
		IO Disable	7		OFF				
C3	PG8	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RTS	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT8	6		I				
		IO Disable	7		OFF				
E3	PG9	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_CTS	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT9	6		I				
		IO Disable	7		OFF				
M3	PG10	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_SYNC	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT10	6		I				
		IO Disable	7		OFF				
D2	PG11	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_CLK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT11	6		I				
		IO Disable	7		OFF				
D1	PG12	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_DOUT	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT12	6		I				
		IO Disable	7		OFF				
B1	PG13	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		PCM1_DIN	2		I				
		Reserved	3		NA				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		PG_EINT13	6		I				
		IO Disable	7		OFF				
H7	VCC-PG	VCC-PG	NA	NA	P	NA	NA	NA	NA
GPIO L									
N1	PL0	Input	0	Function7	I	PU	PU/PD	20	VCC-RTC
		Output	1		O				
		S_TWI_SCK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT0	6		I				
		IO Disable	7		OFF				
M1	PL1	Input	0	Function7	I	PU	PU/PD	20	VCC-RTC
		Output	1		O				
		S_TWI_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT1	6		I				
		IO Disable	7		OFF				
P2	PL2	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_UART_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT2	6		I				
		IO Disable	7		OFF				
R1	PL3	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_UART_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT3	6		I				
		IO Disable	7		OFF				
N2	PL4	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_JTAG_MS	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT4	6		I				
		IO Disable	7		OFF				
R2	PL5	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_JTAG_CK	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT5	6		I				
		IO Disable	7		OFF				
T4	PL6	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_JTAG_DO	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT6	6		I				
		IO Disable	7		OFF				
T3	PL7	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Output	1		O				
		S_JTAG_DI	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT7	6		I				
		IO Disable	7		OFF				
T2	PL8	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT8	6		I				
		IO Disable	7		OFF				
M6	PL9	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT9	6		I				
		IO Disable	7		OFF				
V2	PL10	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_PWM	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT10	6		I				
		IO Disable	7		OFF				
U2	PL11	Input	0	Function7	I	Z	PU/PD	20	VCC-RTC
		Output	1		O				
		S_CIR_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT11	6		I				
		IO Disable	7		OFF				
System									
AA6	NMI	NMI	NA	NA	I	Z	PU/PD	NA	VCC-RTC
V6	RESET	RESET	NA	NA	I/O	Z	PU/PD	NA	VCC-RTC
T5	TEST	TEST	NA	NA	I	PD	PU/PD	NA	VCC-RTC
W6	UBOOT	UBOOT	NA	NA	I	PU	PU/PD	NA	VCC-RTC
A1	JTAG-SEL0	JTAG-SEL0	NA	NA	I	PU	PU/PD	NA	VCC-IO
B2	JTAG-SEL1	JTAG-SEL1	NA	NA	I	PU	PU/PD	NA	VCC-IO
ADC									
AA5	KEYADC	KEYADC	NA	NA	AI	NA	NA	NA	AVCC
TV-OUT									
F10	TVOUT	TVOUT	NA	NA	AO	NA	NA	NA	V33-TV
G9	V33-TV	V33-TV	NA	NA	P	NA	NA	NA	NA
EPHY									
A2	EPHY-LINK-LED	EPHY-LINK-LED	NA	NA	O	NA	NA	NA	EPHY-VCC
F7	EPHY-SPD-LED	EPHY-SPD-LED	NA	NA	O	NA	NA	NA	EPHY-VCC
F6	EPHY-RTX	EPHY-RTX	NA	NA	AI	NA	NA	NA	EPHY-VCC
A4	EPHY-RXN	EPHY-RXN	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
B4	EPHY-RXP	EPHY-RXP	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
A3	EPHY-TXN	EPHY-TXN	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
B3	EPHY-TXP	EPHY-TXP	NA	NA	A I/O	NA	NA	NA	EPHY-VCC
G7	EPHY-VCC	EPHY-VCC	NA	NA	P	NA	NA	NA	NA
F8	EPHY-VDD	EPHY-VDD	NA	NA	P	NA	NA	NA	NA
HDMI									

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
G5	HCEC	HCEC	NA	NA	I/O	NA	NA	NA	VCC-HDMI
M2	HHPD	HHPD	NA	NA	I/O	NA	NA	NA	VCC-HDMI
H3	HSCL	HSCL	NA	NA	O	NA	NA	NA	VCC-HDMI
K3	HSDA	HSDA	NA	NA	I/O	NA	NA	NA	VCC-HDMI
G1	HTX0P	HTX0P	NA	NA	AO	NA	NA	NA	VCC-HDMI
F1	HTX0N	HTX0N	NA	NA	AO	NA	NA	NA	VCC-HDMI
H2	HTXIP	HTXIP	NA	NA	AO	NA	NA	NA	VCC-HDMI
G2	HTX1N	HTX1N	NA	NA	AO	NA	NA	NA	VCC-HDMI
J1	HTX2P	HTX2P	NA	NA	AO	NA	NA	NA	VCC-HDMI
J2	HTX2N	HTX2N	NA	NA	AO	NA	NA	NA	VCC-HDMI
F2	HTXCP	HTXCP	NA	NA	AO	NA	NA	NA	VCC-HDMI
E2	HTXCN	HTXCN	NA	NA	AO	NA	NA	NA	VCC-HDMI
J6	HVCC	VCC-HDMI	NA	NA	P	NA	NA	NA	NA
USB									
B5	USB-DM0	USB-DM0	NA	NA	A I/O	NA	NA	NA	VCC-USB
A5	USB-DP0	USB-DP0	NA	NA	A I/O	NA	NA	NA	VCC-USB
B7	USB-DM1	USB-DM1	NA	NA	A I/O	NA	NA	NA	VCC-USB
B6	USB-DP1	USB-DP1	NA	NA	A I/O	NA	NA	NA	VCC-USB
A8	USB-DM2	USB-DM2	NA	NA	A I/O	NA	NA	NA	VCC-USB
A7	USB-DP2	USB-DP2	NA	NA	A I/O	NA	NA	NA	VCC-USB
B9	USB-DM3	USB-DM3	NA	NA	A I/O	NA	NA	NA	VCC-USB
B8	USB-DP3	USB-DP3	NA	NA	A I/O	NA	NA	NA	VCC-USB
G11	VCC-USB	VCC-USB	NA	NA	P	NA	NA	NA	NA
Audio Codec									
U3	AGND	AGND	NA	NA	G	NA	NA	NA	NA
V3	AVCC	AVCC	NA	NA	P	NA	NA	NA	NA
W1	LINEINR	LINEINR	NA	NA	AI	NA	NA	NA	AVCC
V1	LINEINL	LINEINL	NA	NA	AI	NA	NA	NA	AVCC
Y3	LINEOUTR	LINEOUTR	NA	NA	AO	NA	NA	NA	AVCC
AA3	LINEOUTL	LINEOUTL	NA	NA	AO	NA	NA	NA	AVCC
W3	MBIAS	MBIAS	NA	NA	AO	NA	NA	NA	AVCC
Y1	MICIN1N	MICIN1N	NA	NA	AI	NA	NA	NA	AVCC
W2	MICIN1P	MICIN1P	NA	NA	AI	NA	NA	NA	AVCC
AA2	MICIN2N	MICIN2N	NA	NA	AI	NA	NA	NA	AVCC
Y2	MICIN2P	MICIN2P	NA	NA	AI	NA	NA	NA	AVCC
Y4	VRA1	VRA1	NA	NA	AO	NA	NA	NA	AVCC
W5	VRA2	VRA2	NA	NA	AO	NA	NA	NA	AVCC
V4	VRP	VRP	NA	NA	AO	NA	NA	NA	AVCC
Clock									
V5	X32KIN	X32KIN	NA	NA	AI	NA	NA	NA	VCC-RTC
U4	X32KOUT	X32KOUT	NA	NA	AO	NA	NA	NA	VCC-RTC
P3	X32KFOUT	X32KFOUT	NA	NA	AOD	NA	NA	NA	VCC-RTC
M4	RTC-VIO	RTC-VIO	NA	NA	AO	NA	NA	NA	VCC-RTC
K6	VCC-RTC	VCC-RTC	NA	NA	P	NA	NA	NA	NA
K2	X24MIN	X24MIN	NA	NA	AI	NA	NA	NA	VCC-PLL
K1	X24MOUT	X24MOUT	NA	NA	AO	NA	NA	NA	VCC-PLL
K4	X24MFOUT	X24MFOUT	NA	NA	AOD	NA	NA	NA	VCC-RTC
L5	PLLTEST	PLLTEST	NA	NA	AOD	NA	NA	NA	VCC-PLL
N3	VCC-PLL	VCC-PLL	NA	NA	P	NA	NA	NA	NA
Efuse									
G10	VDD-EFUSE	VDD-EFUSE	NA	NA	P	NA	NA	NA	NA
H11	VDD-EFUSEBP	VDD-EFUSEBP	NA	NA	O	NA	NA	NA	NA
Power									
J12	VDD-GPUFB	VDD-GPUFB	NA	NA	O	NA	NA	NA	NA
N8,P6,P7,P8,P9, R6,R7,R8,T6,T7, T8,U6,U9	VDD-CPUX	VDD-CPU	NA	NA	P	NA	NA	NA	NA
J7,J8	VDD-CPUS	VDD-CPU	NA	NA	P	NA	NA	NA	NA
H10,J10,J11,K10, K11,K12,L10,L11, L12,L13,L14	VDD-SYS	VDD-SYS	NA	NA	P	NA	NA	NA	NA
G13,G14,H13, H14,J14	VCC-IO	VCC-IO	NA	NA	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
Ground									
A21,AA1,G8,H12,H15,H8,J13,J16,J9,K13,K14,K15,K16,K7,K8,K9,L15,L8,L9,M10,M11,M12,M13,M14,M15,M5,M7,M8,M9,N10,N11,N12,N13,N14,N15,N7,N9,P10,P11,P12,P13,P14,P15,R10,R11,R12,R13,R14,R9,T11,T9	GND	GND	NA	NA	G	NA	NA	NA	NA

3.2. Signal Descriptions

H5 contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 3-1. Table 3-2 shows the detailed function description of every signal based on the different interface.

(1).**Signal Name**: The name of every signal.
(2).**Description**: The detailed function description of every signal.
(3).**Type**: Denotes the signal direction:
I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 3-2. Signal Descriptions

Pin/Signal Name	Description	Type
DRAM		
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQS[3:0]	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O
SDQSB[3:0]	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	O
SCK	DRAM Active-High Clock Signal to the Memory Device	O
SCKB	DRAM Active-Low Clock Signal to the Memory Device	O
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device for Two Chip Select	O
SA[15:0]	DRAM Address Signal to the Memory Device	O
SWE	DRAM Write Enable Strobe to the Memory Device	O
SCAS	DRAM Column Address Strobe to the Memory Device	O
SRAS	DRAM Row Address Strobe to the Memory Device	O
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SBA[2:0]	DRAM Bank Address Signal to the Memory Device	O
SODT[1:0]	DRAM On-Die Termination Output Signal for Two Chip Select	O
SRST	DRAM Reset Signal to the Memory Device	O
SZQ	DRAM ZQ Calibration	AI
SVREF	DRAM Reference Input	P

Pin/Signal Name	Description	Type
VCC-DRAM	DRAM Power Supply	P
System		
UBOOT	UBOOT Mode Select	I
TEST	TEST Signal	I
NMI	Non-Maskable Interrupt	I
RESET	Reset Signal	I/O
JTAG-SEL0	JTAG Mode Select 0	I
JTAG-SEL1	JTAG Mode Select 1	I
PLL&Clock		
X32KFOUT	32KHz Clock Fanout	AOD
X32KIN	Clock Input Of 32KHz Crystal	AI
X32KOUT	Clock Output Of 32KHz Crystal	AO
VCC-RTC	RTC Power Supply	P
REXT	External Reference Register	AI
RTC-VIO	Internal LDO Output Bypass	AO
X24MFOUT	24MHz Clock Fanout	AOD
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
PLLTEST	PLL Test	AOD
VCC-PLL	PLL Power Supply	P
HDMI		
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HHPD	HDMI Hot Plug Detection signal	I/O
HCEC	HDMI Consumer Electronics Control	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
HVCC	HDMI Power Supply	P
USB		
USB-DM0	USB DM Signal	A I/O
USB-DP0	USB DP Signal	A I/O
USB-DM1	USBDM Signal	A I/O
USB-DP1	USB DP Signal	A I/O
USB-DM2	USB DM Signal	A I/O
USB-DP2	USB DP Signal	A I/O
USB-DM3	USB DM Signal	A I/O

Pin/Signal Name	Description	Type
USB-DP3	USB DP Signal	A I/O
VCC-USB	USB Power Supply	P
ADC		
KEYADC	ADC Input for KEY Application	AI
EPHY		
EPHY-RXP	Transceiver Positive Output/Input	A I/O
EPHY-RXN	Transceiver Negative Output/Input	A I/O
EPHY-TXP	Transceiver Positive Output/Input	A I/O
EPHY-TXN	Transceiver Negative Output/Input	A I/O
EPHY-RTX	EPHY External Resistance to Ground	AI
EPHY-LINK-LED	EPHY LINK Up/Down Indicator LED	O
EPHY-SPD-LED	EPHY 10M/100M Indicator LED	O
EPHY-VDD	3.3V Analog Power Supply for EPHY	P
EPHY-VCC	1.1V Analog Power Supply for EPHY	P
TV		
TV-OUT	TV Output	AO
V33-TV	TV Out Power Supply	P
Audio Codec		
LINEINL	LINE-IN Left Channel Input	AI
LINEINR	LINE-IN Right Channel Input	AI
LINEOUTL	LINE-OUT Left Channel Output	AO
LINEOUTR	LINE-OUT Right Channel Output	AO
MBIAS	Master Analog Microphone Bias	AO
MICIN1N	Microphone Negative Input 1	AI
MICIN1P	Microphone Positive Input 1	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN2P	Microphone Positive Input 2	AI
VRA1	Reference Voltage Output	AO
VRA2	Reference Voltage Output	AO
VRP	Reference Voltage Output	AO
AVCC	Analog Power	P
AGND	Analog GND	G
I2S/PCM		
PCM0_SYNC	PCM0 Sync/I2S0 Left and Right Channel Select Clock	I/O
PCM0_CLK	PCM0 Sample Rate Clock/I2S0 Bit Clock	I/O
PCM0_DOUT	I2S0/PCM0 Serial Data Output	O
PCM0_DIN	I2S0/PCM0 Serial Data Input	I
PCM0_MCLK	I2S0/PCM0 Master Clock	O
PCM1_SYNC	PCM1 Sync/I2S1 Left and Right Channel Select Clock	I/O
PCM1_CLK	PCM1 Sample Rate Clock/I2S1 Bit Clock	I/O
PCM1_DOUT	I2S1/PCM1 Serial Data Output	O
PCM1_DIN	I2S1/PCM1 Serial Data Input	I

Pin/Signal Name	Description	Type
OWA		
OWA_OUT	One Wire Audio Output	O
SD/MMC		
SDC0_CMD	Command Signal for SD/TF Card	I/O
SDC0_CLK	Clock for SD/TF Card	O
SDC0_D[3:0]	Data Input and Output for SD/TF Card	I/O
SDC1_CMD	Command Signal for SDIO Wi-Fi	I/O
SDC1_CLK	Clock for SDIO Wi-Fi	O
SDC1_D[3:0]	Data Input and Output for SDIO Wi-Fi	I/O
SDC2_CMD	Command Signal for SD/eMMC	I/O
SDC2_CLK	Clock for SD/eMMC	O
SDC2_D[7:0]	Data Input and Output for SD/eMMC	I/O
SDC2_RST	Reset Signal for SD/eMMC	O
NAND FLASH		
NAND_DQ[7:0]	NAND Flash0 Data Bit [7:0]	I/O
NAND_DQS	NADN Flash Data Strobe	I/O
NAND_WE	NAND Flash Write Enable	O
NAND_RE	NAND Flash chip Read Enable	O
NAND_ALE	NAND Flash Address Latch Enable	O
NAND_CLE	NAND Command Latch Enable	O
NAND_CE[1:0]	NAND Flash Chip Select [1:0]	O
NAND_RB[1:0]	NAND Flash Ready/Busy Bit	I
Interrupt		
PA_EINT[21:0]	GPIO A Interrupt	I
PF_EINT[6:0]	GPIO F Interrupt	I
PG_EINT[13:0]	GPIO G Interrupt	I
S_PL_EINT[11:0]	GPIO L Interrupt	I
PWM		
S_PWM	Pulse Width Modulation Output	O
PWM0	Pulse Width Modulation Output	O
IR		
S_CIR_RX	Consumer IR Data Receive	I
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[7:0]	CSI Data bit [7:0]	I
CSI_SCK	CSI Command Serial Clock Signal	I/O
CSI_SDA	CSI Command Serial Data Signal	I/O
EMAC		
RGMII_RXD3/MII_RXD3 /RMII_NULL	RGMII/MII Receive Data	I

Pin/Signal Name	Description	Type
RGMII_RXD2/MII_RXD2/ RMII_NULL	RGMII/MII Receive Data	I
RGMII_RXD1/MII_RXD1/ RMII_RXD1	RGMII/MII /RMII Receive Data	I
RGMII_RXD0/MII_RXD0/ RMII_RXD0	RGMII/MII /RMII Receive Data	I
RGMII_RXCK/MII_RXCK/ RMII_NULL	RGMII/MII Receive Clock	I
RGMII_RXCTL/MII_RXDV/ RMII_CRS_DV	RGMII Receive Control/MII Receive Enable/RMII Carrier Sense-Receive Data Valid	I
RGMII_NULL/MII_RXERR/ RMII_RXER	MII/RMII Receive Error	I
RGMII_TXD3/MII_TXD3/ RMII_NULL	RGMII/MII Transmit Data	O
RGMII_TXD2/MII_TXD2/ RMII_NULL	RGMII/MII Transmit Data	O
RGMII_TXD1/MII_TXD1/ RMII_TXD1	RGMII/MII /RMII Transmit Data	O
RGMII_TXD0/MII_TXD0/ RMII_TXD0	RGMII/MII /RMII Transmit Data	O
RGMII_NULL/MII_CRS/ RMII_NULL	MII Carrier Sense	I
RGMII_TXCK/MII_TXCK/ RMII_TXCK	RGMII/MII /RMII Transmit Clock: Output Pin for RGMII, Input Pin for MII/RMII	I/O
RGMII_TXCTL/MII_TXEN/ RMII_TXEN	RGMII Transmit Control/MII Transmit Enable/RMII Transmit Enable: Output Pin for RGMII/RMII, Input Pin for MII	I/O
RGMII_NULL/MII_TXERR/ RMII_NULL	MII Transmit Error	O
RGMII_CLKIN/MII_COL/ RMII_NULL	RGMII Transmit Clock from External/MII Collision Detect	I
MDC	RGMII/MII /RMII Management Data Clock	O
MDIO	RGMII/MII /RMII Management Data Input/Output	I/O
Transport Stream Controller		
TS0_CLK	Transport Stream0 Clock	I
TS0_ERR	Transport Stream0 Error Indicate	I
TS0_SYNC	Transport Stream0 Sync	I
TS0_DVLD	Transport Stream0 Valid Signal	I
TS0_D[7:0]	Transport Stream0 Data	I
TS1_CLK	Transport Stream1 Clock	I
TS1_ERR	Transport Stream1 Error Indicate	I
TS1_SYNC	Transport Stream1 Sync	I
TS1_DVLD	Transport Stream1 Valid Signal	I
TS1_D0	Transport Stream1 Data	I
TS2_CLK	Transport Stream2 Clock	I
TS2_ERR	Transport Stream2 Error Indicate	I
TS2_SYNC	Transport Stream2 Sync	I
TS2_DVLD	Transport Stream2 Valid Signal	I
TS2_D[7:0]	Transport Stream2 Data	I
TS3_CLK	Transport Stream3 Clock	I
TS3_ERR	Transport Stream3 Error Indicate	I
TS3_SYNC	Transport Stream3 Sync	I
TS3_DVLD	Transport Stream3 Valid Signal	I

Pin/Signal Name	Description	Type
TS3_D0	Transport Stream3 Data	I
SPI (x=[1:0])		
SPIx_CS	SPIx Chip Select signal, Low Active	I/O
SPIx_CLK	SPIx Clock Signal	I/O
SPIx_MOSI	SPIx Master Data Out, Slave Data In	I/O
SPIx_MISO	SPIx Master Data In, Slave Data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear To Send	I
UART1_RTS	UART1 Data Request To Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear To Send	I
UART2_RTS	UART2 Data Request To Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear To Send	I
UART3_RTS	UART3 Data Request To Send	O
S_UART_TX	UART Data Transmit	O
S_UART_RX	UART Data Receive	I
TWI (x=[2:0])		
TWIx_SCK	TWIx Serial Clock Signal	I/O
TWIx_SDA	TWIx Serial Data Signal	I/O
S_TWI_SCK	TWI Serial Clock Signal for CPUs	I/O
S_TWI_SDA	TWI Serial Data Signal for CPUs	I/O
Smart Card Reader(x=[1:0])		
SIMx_PWREN	Smart Card Power Enable	O
SIMx_CLK	Smart Card Clock	O
SIMx_DATA	Smart Card Data	I/O
SIMx_RST	Smart Card Reset	O
SIMx_DET	Smart Card Detect	I
SIMx_VPPEN	Smart Card Program Voltage Enable	O
SIMx_VPPPP	Smart Card Program Control	O
DI		
DI_TX	De-Interlacer Output	O
DI_RX	De-Interlacer Input	I
JTAG		
JTAG_MS	JTAG Mode Select Input	I
JTAG_CK	JTAG Clock Input	I

Pin/Signal Name	Description	Type
JTAG_DO	JTAG Data Output	O
JTAG_DI	JTAG Data Input	I
S_JTAG_MS	JTAG Mode Select Input for CPUs	I
S_JTAG_CK	JTAG Clock Input for CPUs	I
S_JTAG_DO	JTAG Data Output for CPUs	O
S_JTAG_DI	JTAG Data Input for CPUs	I

Chapter 4 System

The chapter describes the H5 system from following sections:

4.1. Memory Mapping

Module	Address (It is for Cluster CPU)	Size (byte)
N-BROM	0x0000 0000—0x0000 7FFF	32K
S-BROM	0x0000 0000—0x0000 FFFF	64K
SRAM A1	0x0001 0000---0x0001 7FFF	32K
SRAM C	0x0001 8000---0x0003 3FFF	112K
SRAM A2	0x0004 4000---0x0005 3FFF	64K
DE	0x0100 0000---0x013F FFFF	4M
Coresight Debug	0x0140 0000---0x0141 FFFF	128K
CPU MBIST	0x0150 2000---0x0150 2FFF	4K
CPU CFG	0x0170 0000---0x0170 03FF	1K
System Control	0x01C0 0000---0x01C0 0FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
NFDC	0x01C0 3000---0x01C0 3FFF	4K
TSC	0x01C0 6000---0x01C0 6FFF	4K
Key Memory Space	0x01C0 B000---0x01C0 BFFF	4K
TCON 0	0x01C0 C000---0x01C0 CFFF	4K
TCON 1	0x01C0 D000---0x01C0 DFFF	4K
VE	0x01C0 E000---0x01C0 EFFF	4K
SMHC 0	0x01C0 F000---0x01C0 FFFF	4K
SMHC 1	0x01C1 0000---0x01C1 0FFF	4K
SMHC 2	0x01C1 1000---0x01C1 1FFF	4K
SID	0x01C1 4000---0x01C1 43FF	1K
Crypto Engine	0x01C1 5000---0x01C1 5FFF	4K
MSG_BOX	0x01C1 7000---0x01C1 7FFF	4K
SPINLOCK	0x01C1 8000---0x01C1 8FFF	4K
USB-OTG_Device	0x01C1 9000---0x01C1 9FFF	4K
USB-OTG_EHCI0/OHCI0	0x01C1 A000---0x01C1 AFFF	4K
USB-HCI1	0x01C1 B000---0x01C1 BFFF	4K
USB-HCI2	0x01C1 C000---0x01C1 CFFF	4K
USB-HCI3	0x01C1 D000---0x01C1 DFFF	4K
SMC	0x01C1 E000---0x01C1 EFFF	4K
CCU	0x01C2 0000---0x01C2 03FF	1K
PIO	0x01C2 0800---0x01C2 0BFF	1K
TIMER	0x01C2 0C00---0x01C2 0FFF	1K
OWA	0x01C2 1000---0x01C2 13FF	1K
PWM	0x01C2 1400---0x01C2 17FF	1K
KEYADC	0x01C2 1800---0x01C2 1BFF	1K
I2S/PCM 0	0x01C2 2000---0x01C2 23FF	1K
I2S/PCM 1	0x01C2 2400---0x01C2 27FF	1K

I2S/PCM 2	0x01C2 2800---0x01C2 2BFF	1K
Audio Codec	0x01C2 2C00---0x01C2 33FF	2K
SPC	0x01C2 3400---0x01C2 37FF	1K
THS	0x01C2 5000---0x01C2 53FF	1K
UART 0	0x01C2 8000---0x01C2 83FF	1K
UART 1	0x01C2 8400---0x01C2 87FF	1K
UART 2	0x01C2 8800---0x01C2 8BFF	1K
UART 3	0x01C2 8C00---0x01C2 8FFF	1K
TWI 0	0x01C2 AC00---0x01C2 AFFF	1K
TWI 1	0x01C2 B000---0x01C2 B3FF	1K
TWI 2	0x01C2 B400---0x01C2 B7FF	1K
SCR0	0x01C2 C400---0x01C2 C7FF	1K
SCR1	0x01C2 C800---0x01C2 CBFF	1K
EMAC	0x01C3 0000---0x01C3 FFFF	64K
HSTMR	0x01C6 0000---0x01C6 0FFF	4K
DRAMCOM	0x01C6 2000---0x01C6 2FFF	4K
DRAMCTL0	0x01C6 3000---0x01C6 3FFF	4K
DRAMPHY0	0x01C6 5000---0x01C6 5FFF	4K
SPI0	0x01C6 8000---0x01C6 8FFF	4K
SPI1	0x01C6 9000---0x01C6 9FFF	4K
SCU	0x01C80000 GIC_DIST: 0x01C80000 + 0x1000 GIC_CPUIF:0x01C80000 + 0x2000	
CSI	0x01CB 0000---0x01CF FFFF	320K
De-interlacer	0x01E0 0000---0x01E1 FFFF	128K
TVE	0x01E4 0000---0x01E4 FFFF	64K
GPU	0x01E8 0000---0x01EA FFFF	192K
HDMI	0x01EE 0000---0x01EF FFFF	128K
RTC	0x01F0 0000---0x01F0 03FF	1K
R_TIMER	0x01F0 0800---0x01F0 0BFF	1K
R_INTC	0x01F0 0C00---0x01F0 0FFF	1K
R_WDOG	0x01F0 1000---0x01F0 13FF	1K
R_PRCM	0x01F0 1400---0x01F0 17FF	1K
R_TWD	0x01F0 1800---0x01F0 1BFF	1K
R_CPUCFG	0x01F0 1C00---0x01F0 1FFF	1K
R_CIR-RX	0x01F0 2000---0x01F0 23FF	1K
R_TWI	0x01F0 2400---0x01F0 27FF	1K
R_UART	0x01F0 2800---0x01F0 2BFF	1K
R_PIO	0x01F0 2C00---0x01F0 2FFF	1K
R_PWM	0x01F0 3800---0x01F0 3BFF	1K
DDR	0x4000 0000---0xFFFF FFFF	3G

4.2. Boot System

4.2.1. Overview

The Boot System includes the following features:

- The system will boot in different ways based on whether its security features are enabled
- Supports CPU-0 boot process and CPU-0+ boot process
- Supports super standby wakeup process
- Supports mandatory upgrade process through USB OTG
- Supports fast boot process from Raw NAND, eMMC, SD/TF card ,and SPI NOR Flash

4.2.2. Boot Diagram

4.2.2.1. Normal Mode

The system will boot in normal mode or security mode based on whether its security feature are enabled.

Normal mode: The system boot will start from CPU-0 or CPU-0+, and the boot process is illustrated below.

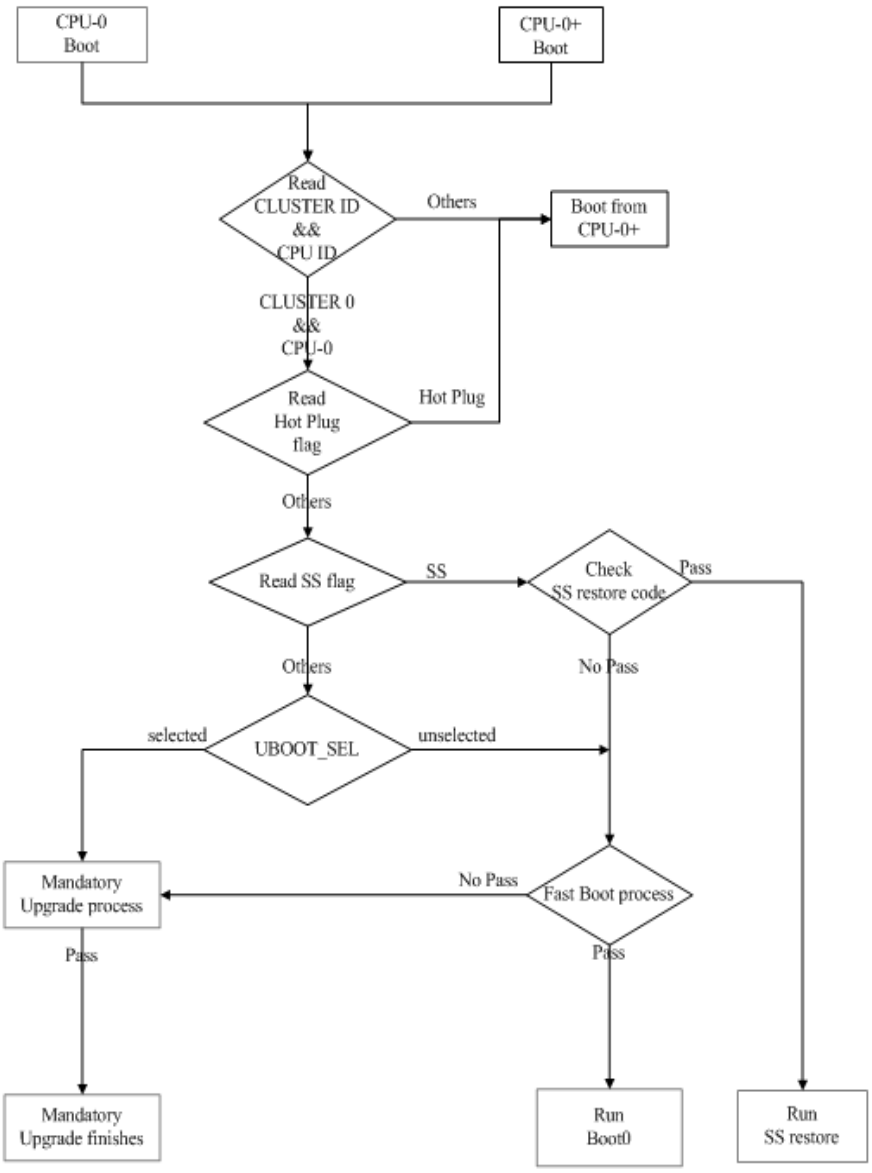


Figure 4-1. Normal Mode Boot Process

CPU-0+: Other CPU cores(CPU1,CPU2,CPU3) except CPU-0

CPU-0+ Boot process: refer to **4.2.2.3.CPU-0+ Boot Process**

CPU Hot Plug process: refer to **4.2.2.4. CPU Hot Plug Process**

Mandatory Upgrade process: refer to **4.2.2.5.Mandatory Upgrade Process**

Fast Boot process: refer to **4.2.2.6. Fast Boot Normal Process** and **4.2.2.7.Fast Boot Security Process**

4.2.2.2. Security Mode

In Security Boot mode, after the fast boot process finishes, the system will go to run Security BROM software.

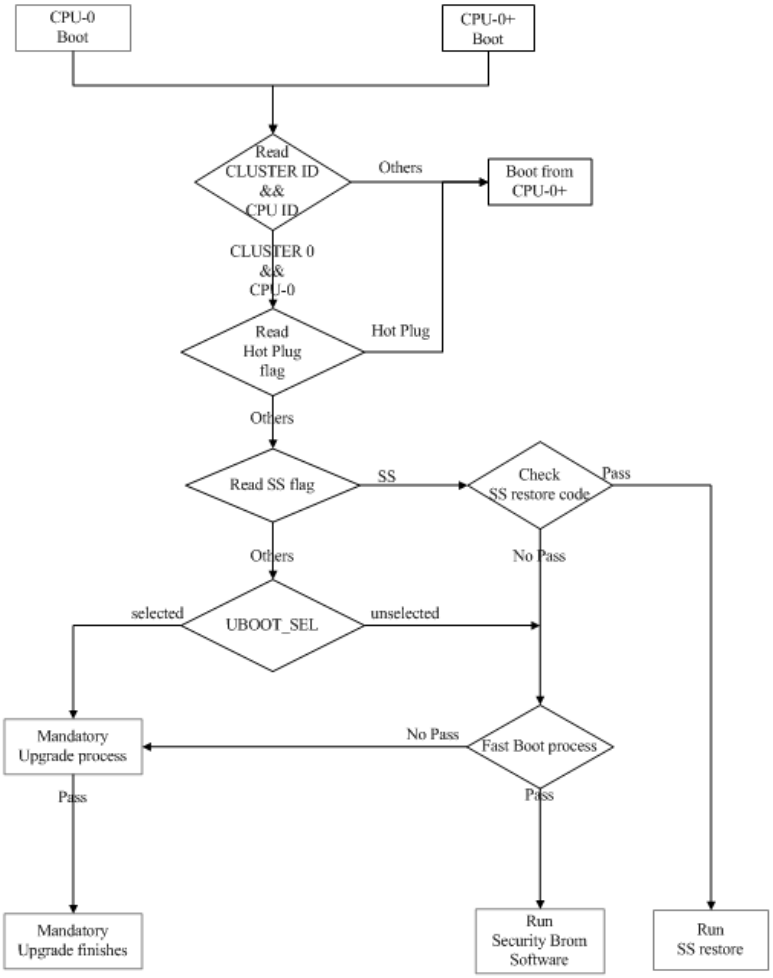


Figure 4-2. Security Mode Boot Process

4.2.2.3. CPU-0+ Boot Process

When the system boots from CPU-0+, BROM will jump to multi-core system firmware address according to the CPU-0+ Boot pointer, and run CPU-0+ boot code.

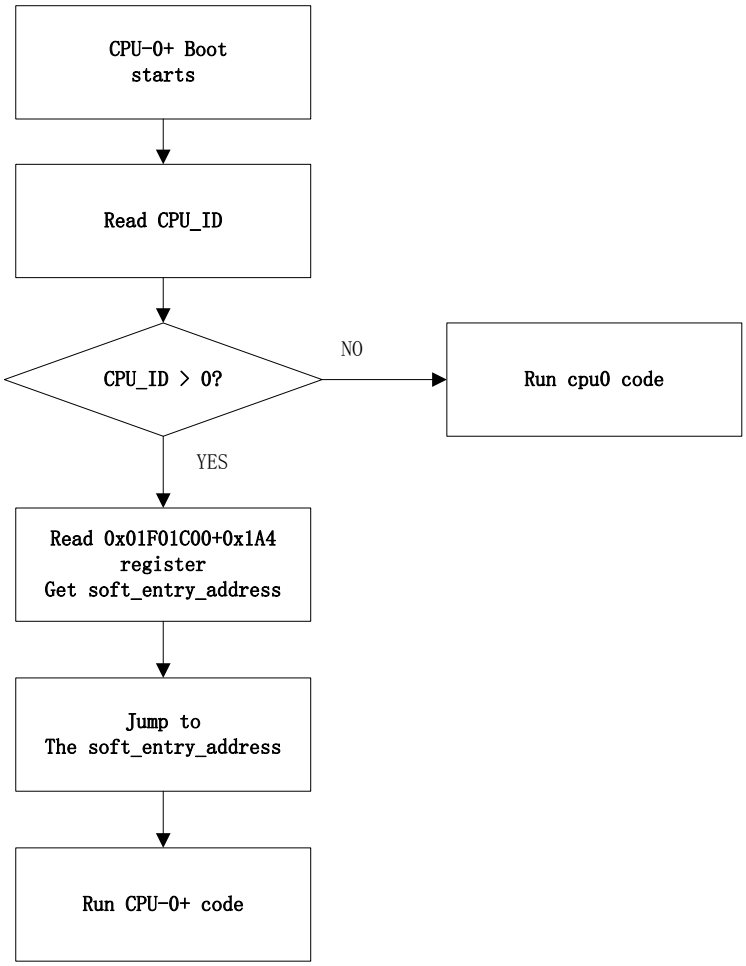


Figure 4-3. CPU-0+ Boot Process

4.2.2.4. CPU Hot Plug Process

The Hot Plug bit determines whether the system will do hot plug boot.

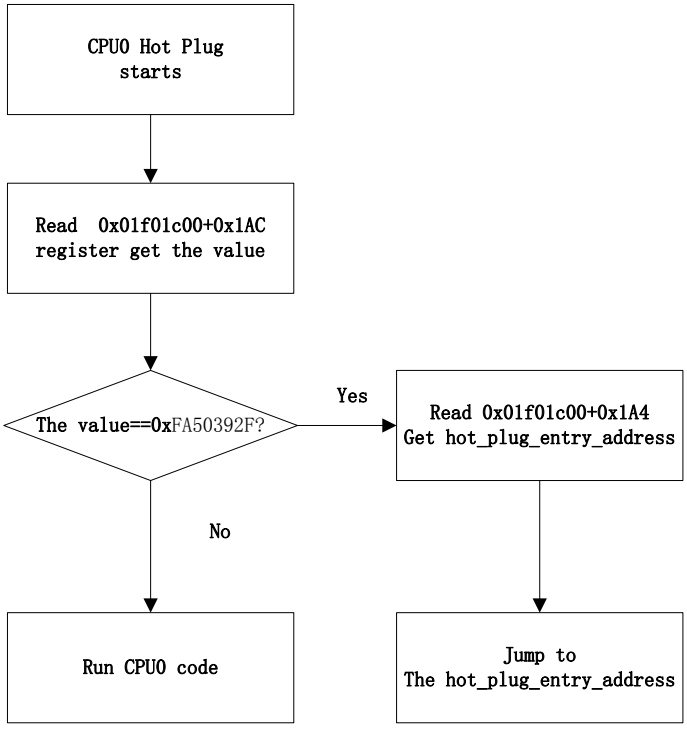


Figure 4-4. CPU Hot Plug Process

4.2.2.5. Super Standby Wakeup Process

Super Standby(SS) wakeup will be started by CPU-S, and will be carried on by CPU-0 after the release of CPU-0.

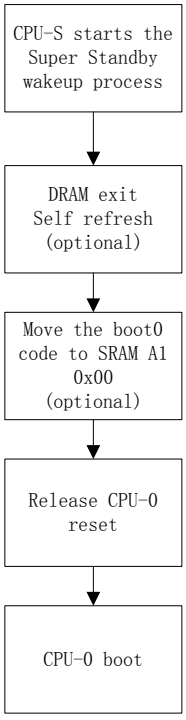


Figure 4-5. Super Standby Wakeup Process

4.2.2.6. Mandatory Upgrade Process

When the system chooses to whether enter mandatory upgrade processor, if the UBOOT_SEL(UBOOT signal) is detected to pull low, then the system will jump to mandatory upgrade process. The mandatory upgrade process is illustrated below.

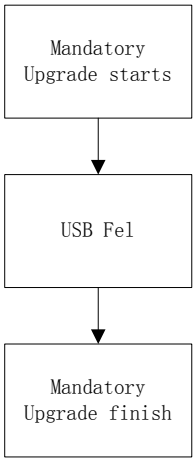


Figure 4-6. Mandatory Upgrade Process

4.2.2.7. Fast Boot Normal Process

When the system chooses to whether enter mandatory upgrade process, if the UBOOT_SEL(UBOOT signal) is detected to pull high, then the system will jump to fast boot process. The fast boot normal process is illustrated below.

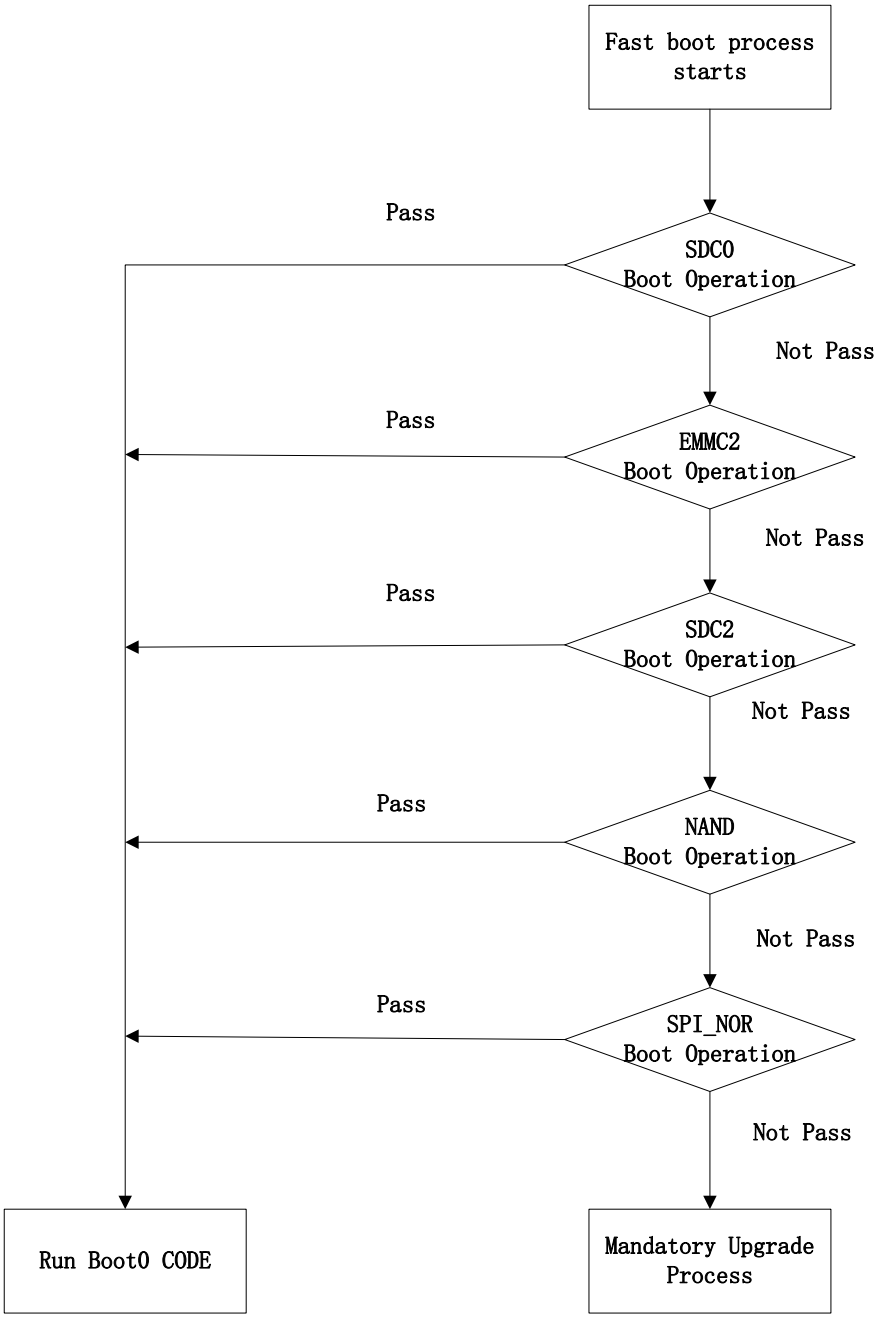


Figure 4-7. Fast Boot Normal Process

4.2.2.8. Fast Boot Security Process

When the system chooses to whether enter mandatory MP process, if the UBOOT_SEL(UBOOT signal) is detected to

pulled to high level, then the system will jump to fast boot process. The fast boot process is illustrated below.

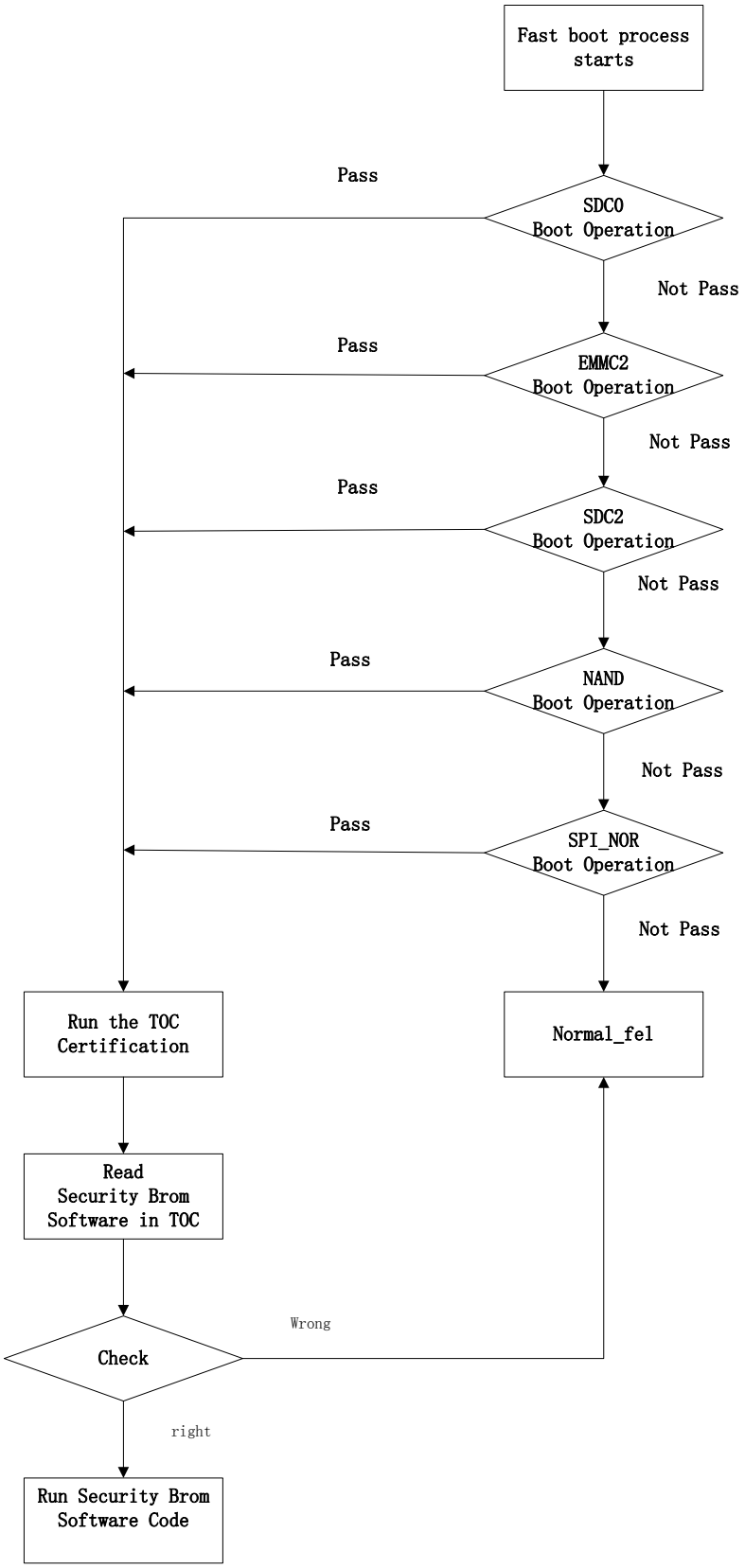


Figure 4-8. Fast Boot Security Process

4.3. CCU

4.3.1. Overview

The CCU controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to other blocks in the system.

Features:

- 9 PLLs, independent PLL for CPUX
- Bus Source and Divisions
- PLLs Bias Control
- PLLs Tuning Control
- PLLs Pattern Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset

4.3.2. Operations and Functional Descriptions

4.3.2.1. System Bus

Figure 4-9 shows a block diagram of the System Bus.

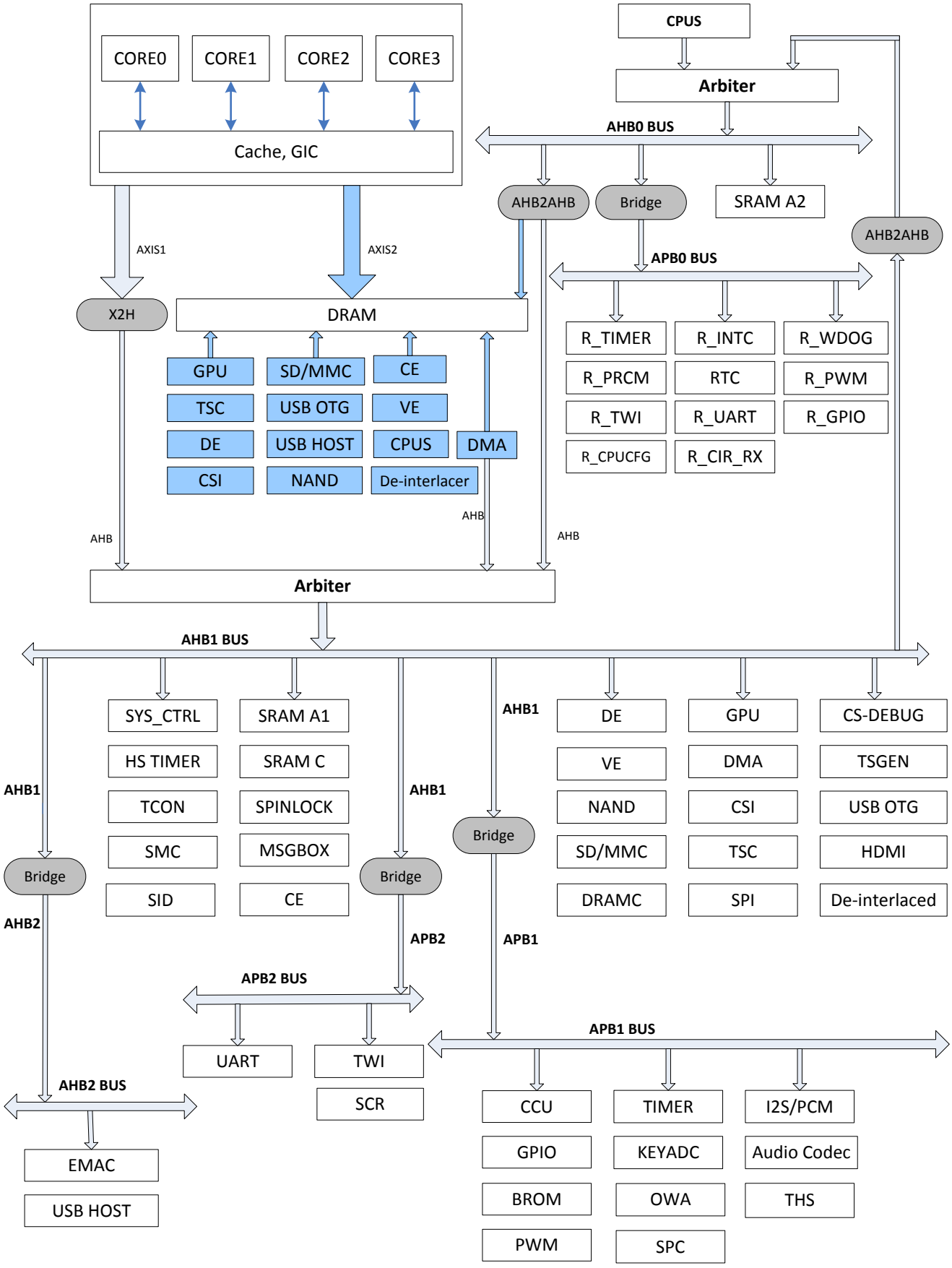


Figure 4-9. System Bus Tree

4.3.2.2. Bus Clock Tree

Figure 4-10 shows a block diagram of the Bus Clock Tree.

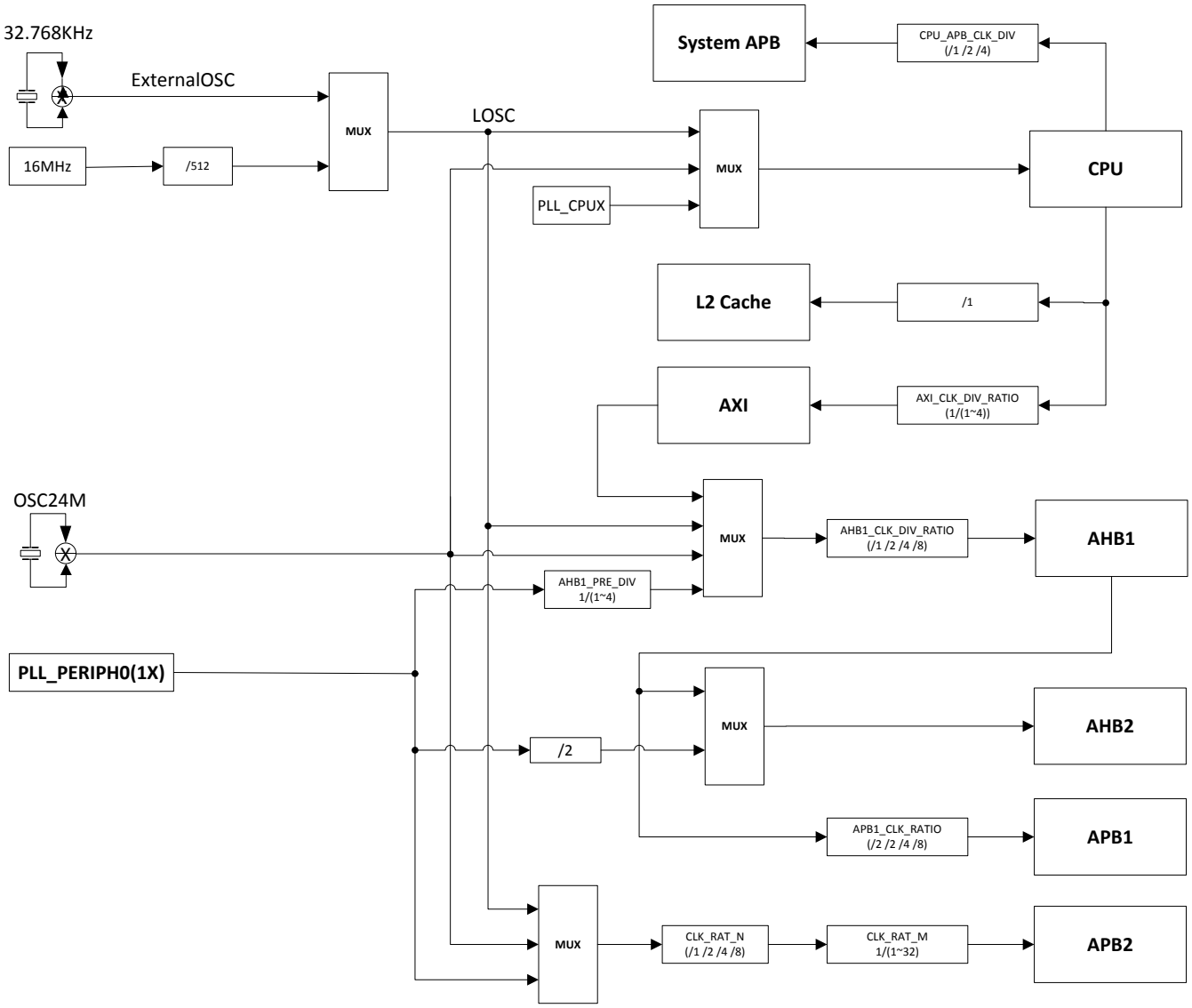


Figure 4-10. Bus Clock Tree

4.3.2.3. Typical Applications

PLL Applications: use the available clock sources to generate clock roots to various parts of the chip. In practical application, other PLLs do not support dynamic frequency scaling except for PLL_CPUX.

Table 4-1. PLLs Typical Applications

PLLs	Typical Applications	Dynamic Frequency Scaling(DFS)
PLL_CPUX	CPU	Support

PLL_AUDIO	I2S/PCM, OWA, Audio Codec Digital Part	Not Support
PLL_VIDEO	TCON,HDMI,CSI,DE2.0	Not Support
PLL_VE	VE	Not Support
PLL_DDR	MBUS,DRAM	Not Support
PLL_PERIPH0	AHB1,AHB2,APB1,APB2,MBUS,NAND,SMHC,CE,SPI,DE2.0,CSI, DEINTERLACE,CPUS	Not Support
PLL_PERIPH1	NAND,SMHC,SPI,TVE,DEINTERLACE,CSI	Not Support
PLL_GPU	GPU	Not Support
PLL_DE	DE,TCON,TVE	Not Support

Note: All module clocks do not support DFS unless other noted. Because when switching module clock source or adjusting division-ratio, the burr or transient instability may be generated, which will hang dead the module.

4.3.2.4. PLL

(1) In practical application, other PLLs do not support dynamic frequency scaling except for PLL_CPUX.
(2) After the PLL_DDR frequency changed, the 20-bit of **PLL_DDR_CTRL_REG** should be written 1 to make it valid.

4.3.2.5. BUS

(1) When setting the BUS clock , you should set the division factor firstly, and after the division factor becomes valid, switch the clock source. The clock source will be switched after at least three clock cycles.
(2) The BUS clock should not be dynamically changed in most applications.

4.3.2.6. Clock Switch

Make sure that the clock source output is valid before the clock source switch, and then set a proper divide ratio; after the division factor becomes valid, switch the clock source.

4.3.2.7. Gating and Reset

Make sure that the reset signal has been released before the release of module clock gating.

4.3.3. Register List

Module Name	Base Address
CCU	0x01C20000

Register Name	Offset	Description

PLL_CPUX_CTRL_REG	0x0000	PLL_CPUX Control Register
PLL_AUDIO_CTRL_REG	0x0008	PLL_AUDIO Control Register
PLL_VIDEO_CTRL_REG	0x0010	PLL_VIDEO Control Register
PLL_VE_CTRL_REG	0x0018	PLL_VE Control Register
PLL_DDR_CTRL_REG	0x0020	PLL_DDR Control Register
PLL_PERIPH0_CTRL_REG	0x0028	PLL_PERIPH0 Control Register
PLL_GPU_CTRL_REG	0x0038	PLL_GPU Control Register
PLL_PERIPH1_CTRL_REG	0x0044	PLL_PERIPH1 Control Register
PLL_DE_CTRL_REG	0x0048	PLL_DE Control Register
CPUX_AXI_CFG_REG	0x0050	CPUX/AXI Configuration Register
AHB1_APB1_CFG_REG	0x0054	AHB1/APB1 Configuration Register
APB2 _CFG_REG	0x0058	APB2 Configuration Register
AHB2_CFG_REG	0x005C	AHB2 Configuration Register
BUS_CLK_GATING_REG0	0x0060	Bus Clock Gating Register 0
BUS_CLK_GATING_REG1	0x0064	Bus Clock Gating Register 1
BUS_CLK_GATING_REG2	0x0068	Bus Clock Gating Register 2
BUS_CLK_GATING_REG3	0x006C	Bus Clock Gating Register 3
BUS_CLK_GATING_REG4	0x0070	Bus Clock Gating Register4
THS_CLK_REG	0x0074	THS Clock Register
NAND_CLK_REG	0x0080	NAND Clock Register
SMHC0_CLK_REG	0x0088	SMHC0 Clock Register
SMHC1_CLK_REG	0x008C	SMHC1 Clock Register
SMHC2_CLK_REG	0x0090	SMHC2 Clock Register
TSC_CLK_REG	0x0098	TSC Clock Register
CE_CLK_REG	0x009C	CE Clock Register
SPI0_CLK_REG	0x00A0	SPI0 Clock Register
SPI1_CLK_REG	0x00A4	SPI1 Clock Register
I2S/PCM0_CLK_REG	0x00B0	I2S/PCM0 Clock Register
I2S/PCM1_CLK_REG	0x00B4	I2S/PCM1 Clock Register
I2S/PCM2_CLK_REG	0x00B8	I2S/PCM2 Clock Register
OWA_CLK_REG	0x00C0	OWA Clock Register
USBPHY_CFG_REG	0x00CC	USBPHY Configuration Register
DRAM_CFG_REG	0x00F4	DRAM Configuration Register
MBUS_RST_REG	0x00FC	MBUS Reset Register
DRAM_CLK_GATING_REG	0x0100	DRAM Clock Gating Register
TCON0_CLK_REG	0x0118	TCON0 Clock Register
TVE_CLK_REG	0x0120	TVE Clock Register
DEINTERLACE_CLK_REG	0x0124	DEINTERLACE Clock Register
CSI_MISC_CLK_REG	0x0130	CSI_MISC Clock Register
CSI_CLK_REG	0x0134	CSI Clock Register
VE_CLK_REG	0x013C	VE Clock Register
AC_DIG_CLK_REG	0x0140	AC Digital Clock Register
AVS_CLK_REG	0x0144	AVS Clock Register
HDMI_CLK_REG	0x0150	HDMI Clock Register

HDMI_SLOW_CLK_REG	0x0154	HDMI Slow Clock Register
MBUS_CLK_REG	0x015C	MBUS Clock Register
GPU_CLK_REG	0x01A0	GPU Clock Register
PLL_STABLE_TIME_REG0	0x0200	PLL Stable Time Register 0
PLL_STABLE_TIME_REG1	0x0204	PLL Stable Time Register 1
PLL_CPUX_BIAS_REG	0x0220	PLL_CPUX Bias Register
PLL_AUDIO_BIAS_REG	0x0224	PLL_AUDIO Bias Register
PLL_VIDEO_BIAS_REG	0x0228	PLL_VIDEO Bias Register
PLL_VE_BIAS_REG	0x022C	PLL_VE Bias Register
PLL_DDR_BIAS_REG	0x0230	PLL_DDR Bias Register
PLL_PERIPH0_BIAS_REG	0x0234	PLL_PERIPH0 Bias Register
PLL_GPU_BIAS_REG	0x023C	PLL_GPU Bias Register
PLL_PERIPH1_BIAS_REG	0x0244	PLL_PERIPH1 Bias Register
PLL_DE_BIAS_REG	0x0248	PLL_DE Bias Register
PLL_CPUX_TUN_REG	0x0250	PLL_CPUX Tuning Register
PLL_DDR_TUN_REG	0x0260	PLL_DDR Tuning Register
PLL_CPUX_PAT_CTRL_REG	0x0280	PLL_CPUX Pattern Control Register
PLL_AUDIO_PAT_CTRL_REG0	0x0284	PLL_AUDIO Pattern Control Register
PLL_VIDEO_PAT_CTRL_REG0	0x0288	PLL_VIDEO Pattern Control Register
PLL_VE_PAT_CTRL_REG	0x028C	PLL_VE Pattern Control Register
PLL_DDR_PAT_CTRL_REG0	0x0290	PLL_DDR Pattern Control Register
PLL_GPU_PAT_CTRL_REG	0x029C	PLL_GPU Pattern Control Register
PLL_PERIPH1_PAT_CTRL_REG1	0x02A4	PLL_PERIPH1 Pattern Control Register
PLL_DE_PAT_CTRL_REG	0x02A8	PLL_DE Pattern Control Register
BUS_SOFT_RST_REG0	0x02C0	Bus Software Reset Register 0
BUS_SOFT_RST_REG1	0x02C4	Bus Software Reset Register 1
BUS_SOFT_RST_REG2	0x02C8	Bus Software Reset Register 2
BUS_SOFT_RST_REG3	0x02D0	Bus Software Reset Register 3
BUS_SOFT_RST_REG4	0x02D8	Bus Software Reset Register 4
CCU_SEC_SWITCH_REG	0x02F0	CCU Security Switch Register
PS_CTRL_REG	0x0300	PS Control Register
PS_CNT_REG	0x0304	PS Counter Register

4.3.4. Register Description

4.3.4.1. PLL_CPUX Control Register (Default Value: 0x0000_1000)

Offset: 0x0000			**Register Name: PLL_CPUX_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable

			1: Enable The PLL Output= (24MHz*N*K)/(M*P). The PLL output is for the CPUX Clock. The PLL output clock must be in the range of 200MHz~2.6GHz. Its default value is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:25	/	/	/
24	R/W	0x0	CPUX_SDM_EN. 0: Disable 1: Enable
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIVP PLL Output external divider P 00: /1 01: /2 10: /4 11: / The P factor only uses in the condition that PLL output is less than 288 MHz.
15:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31, N=32
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M. (M=Factor + 1) The range is from 1 to 4.

4.3.4.2. PLL_AUDIO Control Register (Default Value: 0x0003_5514)

Offset: 0x0008			Register Name: PLL_AUDIO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL is for Audio. PLL_AUDIO = (24MHz*N)/(M*P) PLL_AUDIO(8X)= (24MHz*N*2)/M PLL_AUDIO(4X)=PLL_AUDIO(8X)/2 PLL_AUDIO(2X)=PLL_AUDIO(4X)/2 The PLL output clock must be in the range of 20MHz~200MHz. Its default value is 24.571MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable In this case, only the low 4 bits of **PLL_FACTOR_N** are valid (N: The range is from 1 to 16).
23:20	/	/	/
19:16	R/W	0x3	PLL_POSTDIV_P. Post-div factor P (P= Factor+1) The range is from 1 to 16.
15	/	/	/
14:8	R/W	0x55	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 …… Factor=127, N=128
7:5	/	/	/
4:0	R/W	0x14	PLL_PREDIV_M. PLL Pre-div Factor M (M = Factor+1). The range is from 1 to 32.

4.3.4.3. PLL_VIDEO Control Register (Default Value: 0x0300_6207)

Offset: 0x0010			Register Name: PLL_VIDEO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable In the integer mode, the PLL Output = (24MHz***N**)/**M**. In the fractional mode, the PLL Output is selected by **FRAC_CLK_OUT**. In the Clock Control Module, PLL(1X) Output = PLL, PLL(2X) Output = PLL * 2. The PLL output clock must be in the range of 30MHz~600MHz. Its default value is 297MHz.
30	R/W	0x0	PLL_MODE. 0: Manual Mode 1: Auto Mode (Controlled by DE)
29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PREDIV_M** factor must be set to 0). No meaning when **PLL_MODE_SEL** =1. 0: PLL Output = 270MHz 1: PLL Output = 297MHz
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Per Divider **M** should be set to 0.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1

			Factor=1, N=2 Factor=2, N=3 …… Factor=127, N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre-div Factor M (M = Factor+1). The range is from 1 to 16.

4.3.4.4. PLL_VE Control Register (Default Value: 0x0300_6207)

Offset: 0x0018			Register Name: PLL_VE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable In the integer mode, The PLL Output = (24MHz*N)/M. In the fractional mode, the PLL Output is selected by FRAC_CLK_OUT. The PLL output clock must be in the range of 30MHz~600MHz. Its default value is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when PLL_MODE_SEL =0(PLL_PREDIV_M factor must be set to 0). No meaning when PLL_MODE_SEL =1. 0: PLL Output = 270MHz 1: PLL Output = 297MHz
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Per Divider M should be set to 0.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable

			1: Enable
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31, N=32 … Factor=127, N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre Divider M (M = Factor+1). The range is from 1 to 16.

4.3.4.5. PLL_DDR Control Register (Default Value: 0x0000_1000)

Offset: 0x0020			Register Name: PLL_DDR_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable Set **PLL_DDR_CFG_UPDATE** to validate the PLL after this bit is set to 1. The PLL Output = (24MHz*N*K)/M. The PLL output clock must be in the range of 200MHz~2.6GHz. Its default value is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable
23:21	/	/	/
20	R/W	0x0	PLL_DDR_CFG_UPDATE. PLL_DDR Configuration Update. 0: No effect

			1: Validating the PLL_DDR When PLL_DDR changed, this bit should be set to 1 to validate the PLL, otherwise the change would be invalid. And this bit would be cleared automatically after the PLL change is valid.
19:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31, N=32
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K = Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4.

4.3.4.6. PLL_PERIPH0 Control Register (Default Value: 0x0004_1811)

Offset: 0x0028			**Register Name: PLL_PERIPH0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable The PLL Output = 24MHz*N*K/2. The PLL Output should be fixed to 600MHz, it is not recommended to vary this value arbitrarily. In the Clock Control Module, PLL(2X) output= PLL*2 = 24MHz*N*K. The PLL output clock must be in the range of 200MHz~1.8GHz. Its default value is 600MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:26	/	/	/
25	R/W	0x0	PLL_BYPASS_EN.

			PLL Output Bypass Enable. 0: Disable 1: Enable If the bypass is enabled, the PLL output is 24MHz.
24	R/W	0x0	PLL_CLK_OUT_EN. PLL clock Output Enable. 0: Disable 1: Enable
23:19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable When 25MHz crystal is used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal is used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31, N=32
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_M. PLL Factor M (M = Factor + 1) is only valid in plltest debug. The PLL_PERIPH back door clock output =24MHz***N*K/M**. The range is from 1 to 4.

4.3.4.7. PLL_GPU Control Register (Default Value: 0x0300_6207)

Offset: 0x0038			**Register Name: PLL_GPU_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable In the integer mode, The PLL_GPU Output= (24MHz*N)/M. In the fractional mode, the PLL_GPU Output is selected by **FRAC_CLK_OUT**. The PLL output clock must be in the range of 30MHz~600MHz. Its default value is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PRE_DIV_M** factor must be set to 0). No meaning when **PLL_MODE_SEL** =1. 0: PLL Output = 270MHz 1: PLL Output = 297MHz
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode. 1: Integer Mode When in Fractional mode, the Per Divider **M** should be set to 0.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=127, N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL Pre Divider M (M = Factor+1). The range is from 1 to 16.

4.3.4.8. PLL_PERIPH1 Control Register (Default Value: 0x0004_1811)

Offset: 0x0044			Register Name: PLL_PERIPH1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable The PLL Output = 24MHz*N*K/2. The PLL Output should be fixed to 600MHz, it is not recommended to vary this value arbitrarily. In the Clock Control Module, PLL(2X) output= PLL*2 = 24MHz*N*K. The PLL output clock must be in the range of 200MHz~1.8GHz. Its default value is 600MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:26	/	/	/
25	R/W	0x0	PLL_BYPASS_EN. PLL Output Bypass Enable. 0: Disable 1: Enable If the bypass is enabled, the PLL output is 24MHz.
24	R/W	0x0	PLL_CLK_OUT_EN. PLL clock Output Enable. 0: Disable 1: Enable
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable

			When 25MHz crystal used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31, N=32
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_M. PLL Factor M (M = Factor + 1) is only valid in plltest debug. The PLL_PERIPH back door clock output =24MHz***N*K/M**. The range is from 1 to 4.

4.3.4.9. PLL_DE Control Register (Default Value: 0x0300_6207)

Offset: 0x0048			**Register Name: PLL_DE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable In the integer mode, The PLL Output= (24MHz***N**)/**M**. In the fractional mode, the PLL Output is selected by **FRAC_CLK_OUT**. Its default value is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL is stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PRE_DIV_M** factor must be set to 0). No meaning when **PLL_MODE_SEL** =1.

			0: PLL Output=270MHz 1: PLL Output =297MHz
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Pre Divider **M** should be set to 0.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=0x7F, N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL Per Divider M (M = Factor+1). The range is from 1 to 16.

4.3.4.10. CPUX/AXI Configuration Register (Default Value: 0x0001_0000)

Offset: 0x0050			**Register Name: CPUX_AXI_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x1	CPUX_CLK_SRC_SEL. CPUX Clock Source Select. CPUX Clock = Clock Source 00: LOSC 01: OSC24M 1X: PLL_CPUX If the clock source is changed, wait for at most 8 present running clock cycles.
15:10	/	/	/
9:8	R/W	0x0	CPU_APB_CLK_DIV. 00: /1

			01: /2 1X: /4 **Note:** System APB clock source is CPU clock source.
7:2	/	/	/
1:0	R/W	0x0	AXI_CLK_DIV_RATIO. AXI Clock Divide Ratio. AXI Clock source is CPU clock source. 00: /1 01: /2 10: /3 11: /4

4.3.4.11. AHB1/APB1 Configuration Register (Default Value: 0x0000_1010)

Offset: 0x0054			**Register Name: AHB1_APB1_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	AHB1_CLK_SRC_SEL. 00: LOSC 01: OSC24M 10: AXI 11: PLL_PERIPH0(1X)/**AHB1_PRE_DIV**
11:10	/	/	/
9:8	R/W	0x0	APB1_CLK_RATIO. APB1 Clock Divide Ratio. APB1 clock source is AHB1 clock. 00: /2 01: /2 10: /4 11: /8
7:6	R/W	0x0	AHB1_PRE_DIV AHB1 Clock Pre Divide Ratio 00: /1 01: /2 10: /3 11: /4
5:4	R/W	0x1	AHB1_CLK_DIV_RATIO. AHB1 Clock Divide Ratio.

			00: /1 01: /2 10: /4 11: /8
3:0	/	/	/

4.3.4.12. APB2 Configuration Register (Default Value: 0x0100_0000)

Offset: 0x0058			Register Name: APB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x1	APB2_CLK_SRC_SEL. APB2 Clock Source Select 00: LOSC 01: OSC24M 1X: PLL_PERIPH0(1X) This clock is used for some special module apbclk(UART、TWI). Because these modules need special clock rate even if the apb1clk changed.
23:18	/	/	/
17:16	R/W	0x0	CLK_RAT_N Clock Pre Divide Ratio (n) The select clock source is pre-divided by 2^n. 00: /1 01: /2 10: /4 11: /8
15:5	/	/	/
4:0	R/W	0x0	CLK_RAT_M. Clock Divide Ratio (m) The Pre Divide clock is divided by (m+1). The divider M is from 1 to 32.

4.3.4.13. AHB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: AHB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	AHB2_CLK_CFG. 00: AHB1 Clock 01: PLL_PERIPH0(1X)/2

			1X: / The default clock source of EMAC,USB HOST is AHB2 Clock.

4.3.4.14. Bus Clock Gating Register0 (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: BUS_CLK_GATING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	USBOHCI3_GATING. Gating Clock for USB OHCI3 0: Mask 1: Pass
30	R/W	0x0	USBOHCI2_GATING. Gating Clock for USB OHCI2 0: Mask 1: Pass
29	R/W	0x0	USBOHCI1_GATING. Gating Clock for USB OHCI1 0: Mask 1: Pass
28	R/W	0x0	USB OTG_OHCI0_GATING. Gating Clock for USB OTG_OHCI0 0: Mask 1: Pass
27	R/W	0x0	USBEHCI3_GATING. Gating Clock for USB EHCI3 0: Mask 1: Pass
26	R/W	0x0	USBEHCI2_GATING. Gating Clock for USB EHCI2 0: Mask 1: Pass
25	R/W	0x0	USBEHCI1_GATING. Gating Clock for USB EHCI1 0: Mask 1: Pass
24	R/W	0x0	USB OTG_EHCI0_GATING.

			Gating Clock for USB OTG_EHCI0 0: Mask 1: Pass
23	R/W	0x0	USB OTG_Device_GATING. Gating Clock for USB OTG_Device 0: Mask 1: Pass
22	/	/	/
21	R/W	0x0	SPI1_GATING. Gating Clock for SPI1 0: Mask 1: Pass
20	R/W	0x0	SPI0_GATING. Gating Clock for SPI0 0: Mask 1: Pass
19	R/W	0x0	HSTMR_GATING. Gating Clock for High Speed Timer 0: Mask 1: Pass
18	R/W	0x0	TSC_GATING. Gating Clock for TSC 0: Mask 1: Pass
17	R/W	0x0	EMAC_GATING. Gating Clock for EMAC 0: Mask 1: Pass
16:15	/	/	/
14	R/W	0x0	DRAM_GATING. Gating Clock for DRAM 0: Mask 1: Pass
13	R/W	0x0	NAND_GATING. Gating Clock for NAND 0: Mask

			1: Pass
12:11	/	/	/
10	R/W	0x0	MMC2_GATING. Gating Clock for SMHC2 0: Mask 1: Pass
9	R/W	0x0	MMC1_GATING. Gating Clock for SMHC1 0: Mask 1: Pass
8	R/W	0x0	MMC0_GATING. Gating Clock for SMHC0 0: Mask 1: Pass
7	/	/	/
6	R/W	0x0	DMA_GATING. Gating Clock for DMA 0: Mask 1: Pass
5	R/W	0x0	CE_GATING. Gating Clock for CE. 0: Mask 1: Pass
4:0	/	/	/

4.3.4.15. Bus Clock Gating Register1 (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: BUS_CLK_GATING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	SPINLOCK_GATING. Gating Clock for SPINLOCK 0: Mask 1: Pass.
21	R/W	0x0	MSGBOX_GATING. Gating Clock for MSGBOX 0: Mask

			1: Pass.
20	R/W	0x0	GPU_GATING. Gating Clock for GPU 0: Mask 1: Pass.
19:13	/	/	/
12	R/W	0x0	DE_GATING. Gating Clock for DE 0: Mask 1: Pass.
11	R/W	0x0	HDMI_GATING. Gating Clock for HDMI 0: Mask 1: Pass.
10	/	/	/
9	R/W	0x0	TVE_GATING. Gating Clock for TVE 0: Mask 1: Pass.
8	R/W	0x0	CSI_GATING. Gating Clock for CSI 0: Mask 1: Pass.
7:6	/	/	/
5	R/W	0x0	DEINTERLACE_GATING. Gating Clock for DEINTERLACE 0: Mask 1: Pass
4	R/W	0x0	TCON1_GATING. Gating Clock for TCON1 0: Mask 1: Pass.
3	R/W	0x0	TCON0_GATING. Gating Clock for TCON0 0: Mask 1: Pass.
2:1	/	/	/

0	R/W	0x0	VE_GATING. Gating Clock for VE 0: Mask 1: Pass.

4.3.4.16. Bus Clock Gating Register2 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: BUS_CLK_GATING_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	I2S/PCM2_GATING. Gating Clock for I2S/PCM2 0: Mask 1: Pass.
13	R/W	0x0	I2S/PCM1_GATING. Gating Clock for I2S/PCM1 0: Mask 1: Pass.
12	R/W	0x0	I2S/PCM0_GATING. Gating Clock for I2S/PCM0 0: Mask 1: Pass.
11:9	/	/	/
8	R/W	0x0	THS_GATING. Gating Clock for THS 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	PIO_GATING. Gating Clock for Port Controller 0: Mask 1: Pass.
4:2	/	/	/
1	R/W	0x0	OWA_GATING. Gating Clock for OWA 0: Mask 1: Pass.

0	R/W	0x0	AC_DIG_GATING. Gating Clock for Audio Codec Digital Part 0: Mask 1: Pass

4.3.4.17. Bus Clock Gating Register3 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: BUS_CLK_GATING_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	SCR1_GATING. Gating Clock for SCR1 0: Mask 1: Pass
20	R/W	0x0	SCR0_GATING. Gating Clock for SCR0 0: Mask 1: Pass
19	R/W	0x0	UART3_GATING. Gating Clock for UART3 0: Mask 1: Pass.
18	R/W	0x0	UART2_GATING. Gating Clock for UART2 0: Mask 1: Pass.
17	R/W	0x0	UART1_GATING. Gating Clock for UART1 0: Mask 1: Pass.
16	R/W	0x0	UART0_GATING. Gating Clock for UART0 0: Mask 1: Pass.
15:3	/	/	/
2	R/W	0x0	TWI2_GATING. Gating Clock for TWI2

			0: Mask 1: Pass.
1	R/W	0x0	TWI1_GATING. Gating Clock for TWI1 0: Mask 1: Pass.
0	R/W	0x0	TWI0_GATING. Gating Clock for TWI0 0: Mask 1: Pass.

4.3.4.18. Bus Clock Gating Register4 (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: BUS_CLK_GATING_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DBGSYS_GATING. Gating Clock for DBGSYS 0: Mask 1: Pass
6:1	/	/	/
0	R/W	0x0	EPHY_GATING. Gating Clock for EPHY 0: Mask 1: Pass

4.3.4.19. THS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: THS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock. 0: Clock is OFF 1: Clock is ON This special clock = **THS_CLK_SRC_SEL**/**THS_CLK_DIV_RATIO**.
30:26	/	/	/

25:24	R/W	0x0	THS_CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: / 10: / 11: /
23:2	/	/	/
1:0	R/W	0x0	THS_CLK_DIV_RATIO. THS Clock Divide Ratio. 00: /1 01: /2 10: /4 11: /6

4.3.4.20. NAND Clock Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: NAND_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL**/**CLK_DIV_RATIO_N**/**CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/

3:0	R/W	0x0	CLK_DIV_RATIO_M Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.21. SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL**/**CLK_DIV_RATIO_N**/**CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.22. SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz)

			0: Clock is OFF 1: Clock is ON. SCLK = CLK_SRC_SEL/CLK_DIV_RATIO_N/CLK_DIV_RATIO_M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre-Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.23. SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = CLK_SRC_SEL/CLK_DIV_RATIO_N/CLK_DIV_RATIO_M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /

23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.24. TSC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TSC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL**/**CLK_DIV_RATIO_N**/**CLK_DIV_RATIO_M**.
30:28	/	/	/
27:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0000: OSC24M 0001: PLL_PERIPH0(1X) Others: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8. 00: /1 01: /2 10: /4 11: /8
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

4.3.4.25. CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 400MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL**/**CLK_DIV_RATIO_N**/**CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.26. SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.

			SCLK = **CLK_SRC_SEL**/**CLK_DIV_RATIO_N**/**CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.27. SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00A4			**Register Name: SPI1_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK= **CLK_SRC_SEL**/**CLK_DIV_RATIO_N**/**CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n)

			00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.28. I2S/PCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: I2S/PCM0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO(8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO
15:0	/	/	/

4.3.4.29. I2S/PCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: I2S/PCM1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO(8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4

			11: PLL_AUDIO
15:0	/	/	/

4.3.4.30. I2S/PCM2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: I2S/PCM2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO(8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO
15:0	/	/	/

4.3.4.31. OWA Clock Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: OWA_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK= **PLL _AUDIO/CLK_DIV_RATIO_M**.
30:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.32. USBPHY Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: USBPHY_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/

19	R/W	0x0	SCLK_GATING_OHCI3. Gating Special Clock for OHCI3 0: Clock is OFF 1: Clock is ON
18	R/W	0x0	SCLK_GATING_OHCI2. Gating Special Clock for OHCI2 0: Clock is OFF 1: Clock is ON
17	R/W	0x0	SCLK_GATING_OHCI1. Gating Special Clock for OHCI1 0: Clock is OFF 1: Clock is ON
16	R/W	0x0	SCLK_GATING_OTG_OHCI0. Gating Special Clock for USB OTG_OHCI0 0: Clock is OFF 1: Clock is ON
15:12	/	/	/
11	R/W	0x0	SCLK_GATING_USBPHY3. Gating Special Clock for USB PHY3 0: Clock is OFF 1: Clock is ON
10	R/W	0x0	SCLK_GATING_USBPHY2. Gating Special Clock for USB PHY2 0: Clock is OFF 1: Clock is ON
9	R/W	0x0	SCLK_GATING_USBPHY1. Gating Special Clock for USB PHY1 0: Clock is OFF 1: Clock is ON
8	R/W	0x0	SCLK_GATING_USBPHY0. Gating Special Clock for USB PHY0 0: Clock is OFF 1: Clock is ON
7:4	/	/	/
3	R/W	0x0	USBPHY3_RST. USB PHY3 Reset Control

			0: Assert 1: De-assert
2	R/W	0x0	USBPHY2_RST. USB PHY2 Reset Control 0: Assert 1: De-assert.
1	R/W	0x0	USBPHY1_RST. USB PHY1 Reset Control 0: Assert 1: De-assert
0	R/W	0x0	USBPHY0_RST. USB PHY0 Reset Control 0: Assert 1: De-assert

4.3.4.33. DRAM Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: DRAM_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DRAM_CTR_RST. DRAM Controller Reset for AHB Clock Domain. 0: Assert 1: De-assert. SCLK = **CLK_SRC_SEL**/**DRAM_DIV_M**
30:22			
21:20	R/W	0x0	CLK_SRC_SEL. 00: PLL_DDR 01: PLL_PERIPH0(2X) Others: /
19:17	/	/	/
16	R/W	0x0	SDRCLK_UPD. SDRCLK Configuration Update. 0: Invalid 1: Valid. Setting this bit will validate SDRCLK configuration . It will be automatically cleared after the configuration is valid.

			The DRAMCLK Source is from **PLL_DDR**.
15:2	/	/	/
1:0	R/W	0x0	DRAM_DIV_M. DRAMCLK Divider of Configuration. The clock is divided by (m+1). The divider M should be from 1 to 4.

4.3.4.34. MBUS Reset Register (Default Value: 0x8000_0000)

Offset: 0x00FC			Register Name: MBUS_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MBUS_RESET. 0: Reset Mbus Domain 1: Assert Mbus Domain.
30:0	/	/	/

4.3.4.35. DRAM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: DRAM_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	TSC_DCLK_GATING. Gating DRAM Clock for TSC 0: Mask 1: Pass
2	R/W	0x0	DEINTERLACE_DCLK_GATING. Gating DRAM SCLK(1X) for DEINTERLACE 0: Mask 1: Pass
1	R/W	0x0	CSI_DCLK_GATING. Gating DRAM Clock for CSI 0: Mask 1: Pass
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM Clock for VE 0: Mask 1: Pass

4.3.4.36. DE Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = **CLK_SRC_SEL**/**CLK_DIV_RATIO_M**.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_PERIPH0(2X) 001: PLL_DE Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

4.3.4.37. TCON0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: TCON0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: **PLL_VIDEO** Others: /.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.38. TVE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: TVE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK= **CLK_SRC_SEL**/**CLK_DIV_RATIO_M**.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_DE 001: PLL_PERIPH1(1X) Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

4.3.4.39. DEINTERLACE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: DEINTERLACE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = **CLK_SRC_SEL**/**CLK_DIV_RATIO_M**
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_PERIPH0 001: PLL_PERIPH1 Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

4.3.4.40. CSI_MISC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: CSI_MISC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI_MISC_SCLK_GATING. 0: Clock is OFF 1: Clock is ON. This clock = OSC24M.
30:0	/	/	/

4.3.4.41. CSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: CSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK= **SCLK_SRC_SEL**/**CSI_SCLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	SCLK_SRC_SEL. Special Clock Source Select 000: PLL_PERIPH0(1X) 001: PLL_PERIPH1(1X) Others: /
23:20	/	/	/
19:16	R/W	0x0	CSI_SCLK_DIV_M. CSI Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.
15	R/W	0x0	CSI_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON This clock = **MCLK_SRC_SEL**/**CSI_MCLK_DIV_M**.
14:11	/	/	/

10:8	R/W	0x0	MCLK_SRC_SEL. Master Clock Source Select 000: OSC24M 001: PLL_VIDEO 010: PLL_PERIPH1(1X) Others: /
7:5	/	/	/
4:0	R/W	0x0	CSI_MCLK_DIV_M. CSI Master Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

4.3.4.42. VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VE_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = **PLL_VE**/**CLK_DIV_RATIO_N**.
30:19	/	/	/.
18:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (N) The select clock source is pre-divided by (n+1). The divider N is from 1 to 8.
15:0	/	/	/

4.3.4.43. AC Digital Clock Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: AC_DIG_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_1X_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = **PLL _AUDIO** Output.
30:0	/	/	/

4.3.4.44. AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK= OSC24M.
30:0	/	/	/

4.3.4.45. HDMI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: HDMI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK= **SCLK_SEL**/**CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	SCLK_SEL. Special Clock Source Select 00: PLL_VIDEO Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

4.3.4.46. HDMI Slow Clock Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: HDMI_SLOW_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HDMI_DDC_CLK_GATING. 0: Clock is OFF 1: Clock is ON.

			SCLK = OSC24M.
30:0	/	/	/

4.3.4.47. MBUS Clock Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: MBUS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS 0: Clock is OFF 1: Clock is ON. MBUS_CLOCK = **MBUS_SCLK_SRC**/**MBUS_SCLK_RATIO_M**
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_DDR 11: /.
23:3	/	/	/
2:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 8. **Note:** If the clock has been changed , it must wait for at least 16 cycles.

4.3.4.48. GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x01A0			Register Name: GPU_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. 0: Clock is OFF 1: Clock is ON. SCLK= **PLL_GPU**/**CLK_DIV_RATIO_N**.
30:3	/	/	/.
2:0	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (N) The select clock source is pre-divided by (n+1). The divider N is from 1 to 8.

4.3.4.49. PLL Stable Time Register0 (Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: PLL_STABLE_TIME_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x00FF	PLL_LOCK_TIME PLL Lock Time (Unit: us). **Note:** When any PLL (except PLL_CPU) is enabled or changed, the corresponding PLL lock bit will be set after the PLL Lock Time.

4.3.4.50. PLL Stable Time Register1 (Default Value: 0x0000_00FF)

Offset: 0x0204			Register Name: PLL_STABLE_TIME_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x00FF	PLL_CPU_LOCK_TIME PLL_CPU Lock Time (Unit: us). **Note:** When PLL_CPU is enabled or changed, the PLL_CPU lock bit will be set after the PLL_CPU Lock Time.

4.3.4.51. PLL_CPUX Bias Register (Default Value: 0x0810_0200)

Offset: 0x0220			Register Name: PLL_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VCO_RST. VCO reset in.
30:29	/	/	/
28	R/W	0x0	EXG_MODE. Exchange Mode. CPU PLL source will select **PLL_PERIPH0** instead of **PLL_CPUX**
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0].
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL. PLL Lock Time Control[2:0].
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACT_CTRL. PLL Damping Factor Control[3:0].

4.3.4.52. PLL_AUDIO Bias Register (Default Value: 0x1010_0000)

Offset: 0x0224			Register Name: PLL_AUDIO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias Current[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR. PLL Bias Current[4:0].
15:0	/	/	/

4.3.4.53. PLL_VIDEO Bias Register (Default Value: 0x1010_0000)

Offset: 0x0228			Register Name: PLL_VIDEO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

4.3.4.54. PLL_VE Bias Register (Default Value: 0x1010_0000)

Offset: 0x022C			Register Name: PLL_VE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

4.3.4.55. PLL_DDR Bias Register (Default Value: 0x8110_4000)

Offset: 0x0230			Register Name: PLL_DDR_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x8	PLL_VCO_BIAS. PLL VCO Bias[3:0].
27:26	/	/	/.
25	R/W	0x0	PLL_VCO_GAIN_CTRL_EN. PLL VCO Gain Control Enable. 0: Disable 1: Enable.
24	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide.
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15	/	/	/
14:12	R/W	0x4	PLL_VCO_GAIN_CTRL. PLL VCO Gain Control Bit[2:0].
11:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[3:0].

4.3.4.56. PLL_PERIPH0 Bias Register (Default Value: 0x1010_0010)

Offset: 0x0234			Register Name: PLL_PERIPH0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide
3:2	/	/	/

1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0].

4.3.4.57. PLL_GPU Bias Register (Default Value: 0x1010_0000)

Offset: 0x023C			Register Name: PLL_GPU_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

4.3.4.58. PLL_PERIPH1 Bias Register (Default Value: 0x1010_0010)

Offset: 0x0244			Register Name: PLL_PERIPH1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0].

4.3.4.59. PLL_DE Bias Register (Default Value: 0x1010_0000)

Offset: 0x0248			Register Name: PLL_DE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

4.3.4.60. PLL_CPUX Tuning Register (Default Value: 0x0A10_1000)

Offset: 0x0250			Register Name: PLL_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	PLL_BAND_WID_CTRL. PLL Band Width Control. 0: Narrow 1: Wide
26	R/W	0x0	VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: Disable 1: Enable
25:23	R/W	0x4	VCO_GAIN_CTRL. VCO Gain Control Bits[2:0].
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0].
15	R/W	0x0	C_OD. C-Reg-Od for Verify.
14:8	R/W	0x10	C_B_IN. C-B-In[6:0] for Verify.
7	R/W	0x0	C_OD1. C-Reg-Od1 for Verify.
6:0	R	0x0	C_B_OUT. C-B-Out[6:0] for Verify.

4.3.4.61. PLL_DDR Tuning Register (Default Value: 0x1488_0000)

Offset: 0x0260			Register Name: PLL_DDR_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	VREG1_OUT_EN.

			VREG1 Out Enable. 0: Disable 1: Enable
27	/	/	/
26:24	R/W	0x4	PLL_LTIME_CTRL. PLL Lock Time Control[2:0].
23	R/W	0x1	VCO_RST. VCO Reset In.
22:16	R/W	0x08	PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0].
15	R/W	0x0	OD1. Reg-Od1 for Verify.
14:8	R/W	0x0	B_IN. B-In[6:0] for Verify.
7	R/W	0x0	OD. Reg-Od for Verify.
6:0	R	0x0	B_OUT. B-Out[6:0] for Verify.

4.3.4.62. PLL_CPUX Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PLL_CPUX_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.63. PLL_AUDIO Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PLL_AUDIO_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.64. PLL_VIDEO Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: PLL_VIDEO_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency.

			00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.65. PLL_VE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: PLL_VE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.66. PLL_DDR Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PLL_DDR_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0

			01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.67. PLL_GPU Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: PLL_GPU_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.68. PLL_PERIPH1 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x02A4	Register Name: PLL_PERIPH1_PAT_CTRL_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.69. PLL_DE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PLL_DE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz

16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

4.3.4.70. Bus Software Reset Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name: BUS_SOFT_RST_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	USBOHCI3_RST. USB OHCI3 Reset Control 0: Assert 1: De-assert
30	R/W	0x0	USBOHCI2_RST. USB OHCI2 Reset Control 0: Assert 1: De-assert
29	R/W	0x0	USBOHCI1_RST. USB OHCI1 Reset Control 0: Assert 1: De-assert
28	R/W	0x0	USB OTG_OHCI0_RST. USB OTG_OHCI0 Reset Control 0: Assert 1: De-assert
27	R/W	0x0	USBEHCI3_RST. USB EHCI3 Reset Control 0: Assert 1: De-assert
26	R/W	0x0	USBEHCI2_RST. USB EHCI2 Reset Control 0: Assert 1: De-assert
25	R/W	0x0	USBEHCI1_RST. USB EHCI1 Reset Control 0: Assert 1: De-assert.
24	R/W	0x0	USB OTG_EHCI0_RST. USB OTG_EHCI0 Reset Control

			0: Assert 1: De-assert
23	R/W	0x0	USB OTG_Device_RST. USB OTG_Device Reset Control 0: Assert 1: De-assert
22	/	/	/
21	R/W	0x0	SPI1_RST. SPI1 Reset. 0: Assert 1: De-assert
20	R/W	0x0	SPI0_RST. SPI0 Reset. 0: Assert 1: De-assert
19	R/W	0x0	HSTMR_RST. HSTMR Reset. 0: Assert 1: De-assert
18	R/W	0x0	TSC_RST. TSC Reset. 0: Assert 1: De-assert
17	R/W	0x0	EMAC_RST. EMAC Reset. 0: Assert 1: De-assert
16:15	/	/	/
14	R/W	0x0	SDRAM_RST. SDRAM AHB Reset. 0: Assert 1: De-assert
13	R/W	0x0	NAND_RST. NAND Reset. 0: Assert 1: De-assert

12:11	/	/	/
10	R/W	0x0	SMHC2_RST. SD/MMC2 Reset. 0: Assert 1: De-assert
9	R/W	0x0	SMHC1_RST. SD/MMC1 Reset. 0: Assert 1: De-assert
8	R/W	0x0	SMHC0_RST. SD/MMC0 Reset. 0: Assert 1: De-assert
7	/	/	/
6	R/W	0x0	DMA_RST. DMA Reset. 0: Assert 1: De-assert
5	R/W	0x0	CE_RST. CE Reset. 0: Assert 1: De-assert
4:0	/	/	/

4.3.4.71. Bus Software Reset Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: BUS_SOFT_RST_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBGSYS_RST. DBGSYS Reset. 0: Assert 1: De-assert
30:23	/	/	/
22	R/W	0x0	SPINLOCK_RST. SPINLOCK Reset. 0: Assert 1: De-assert.

21	R/W	0x0	MSGBOX_RST. MSGBOX Reset. 0: Assert 1: De-assert.
20	R/W	0x0	GPU_RST. GPU Reset. 0: Assert 1: De-assert.
19:13	/	/	/
12	R/W	0x0	DE_RST. DE Reset. 0: Assert 1: De-assert.
11	R/W	0x0	HDMI1_RST. HDMI1 Reset. 0: Assert 1: De-assert.
10	R/W	0x0	HDMI0_RST. HDMI0 Reset. 0: Assert 1: De-assert.
9	R/W	0x0	TVE_RST. TVE Reset. 0: Assert 1: De-assert
8	R/W	0x0	CSI_RST. CSI Reset. 0: Assert 1: De-assert.
7:6	/	/	
5	R/W	0x0	DEINTERLACE_RST. DEINTERLACE Reset. 0: Assert 1:De-assert
4	R/W	0x0	TCON1_RST. TCON1 Reset.

			0: Assert 1: De-assert.
3	R/W	0x0	TCON0_RST. TCON0 Reset. 0: Assert 1: De-assert.
2:1	/	/	/
0	R/W	0x0	VE_RST. VE Reset. 0: Assert 1: De-assert.

4.3.4.72. Bus Software Reset Register 2 (Default Value: 0x0000_0000)

Offset: 0x02C8			Register Name: BUS_SOFT_RST_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	EPHY_RST. EPHY Reset. 0: Assert 1: De-assert
1:0	/	/	/

4.3.4.73. Bus Software Reset Register 3 (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: BUS_SOFT_RST_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	I2S/PCM2_RST. I2S/PCM2 Reset. 0: Assert 1: De-assert.
13	R/W	0x0	I2S/PCM1_RST. I2S/PCM1 Reset. 0: Assert 1: De-assert.
12	R/W	0x0	I2S/PCM0_RST. I2S/PCM0 Reset.

			0: Assert 1: De-assert.
11:9	/	/	/
8	R/W	0x0	THS_RST. THS Reset. 0: Assert 1: De-assert
7:2	/	/	/
1	R/W	0x0	OWA_RST. OWA Reset. 0: Assert 1: De-assert
0	R/W	0x0	AC_RST. Audio Codec Reset. 0: Assert 1: De-assert

4.3.4.74. Bus Software Reset Register 4 (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: BUS_SOFT_RST_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	SCR1_RST. SCR1 Reset. 0: Assert 1: De-assert
20	R/W	0x0	SCR0_RST. SCR0 Reset. 0: Assert 1: De-assert
19	R/W	0x0	UART3_RST. UART3 Reset. 0: Assert 1: De-assert.
18	R/W	0x0	UART2_RST. UART2 Reset.

			0: Assert 1: De-assert.
17	R/W	0x0	UART1_RST. UART1 Reset. 0: Assert 1: De-assert.
16	R/W	0x0	UART0_RST. UART0 Reset. 0: Assert 1: De-assert.
15:3	/	/	/
2	R/W	0x0	TWI2_RST. TWI2 Reset. 0: Assert 1: De-assert.
1	R/W	0x0	TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert.
0	R/W	0x0	TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert.

4.3.4.75. CCU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: CCU_SEC_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MBUS_SEC MBUS clock register security 0: Secure 1: Non-secure Including MBUS Reset Register and MBUS Clock Register
1	R/W	0x0	BUS_SEC Bus relevant registers security

			0: Secure 1: Non-secure Including AXI/AHB/APB relevant registers,such as CPUX/AXI Configuration Register,AHB1/APB1 Configuration Register,APB2 Configuration Register, AHB2 Configuration Register.
0	R/W	0x0	PLL_SEC PLL relevant registers security. 0: Secure 1: Non-secure Including PLL_CPUX Control Register,PLL_AUDIO Control Register,PLL_VIDEO Control Register,PLL_VE Control Register,PLL_DDR Control Register, PLL_PEPIPH0 Control Register,PLL_GPU Control Register,PLL_PERIPH1 Control Register,PLL_DE Control Register and offset from 0x200 to 0x2A8 relevant registers.

4.3.4.76. PS Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			**Register Name: PS_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	DEC_SEL Device Select
7	R/W	0x0	DET_FIN. Detect Finish. 0: Unfinished 1: Finished Setting 1 to this bit will clear it.
6	R/W	0x0	DLY_SEL. Delay Select 0: 1 Cycle 1: 2 Cycles
5:4	R/W	0x0	OSC_SEL OSC Select. 00: IDLE 01: SVT 10: LVT 11: ULVT

3:1	R/W	0x0	TIME_DET. Time Detect. 000: 0.5/4 us 001: 0.5/2 us 010: 0.5/1 us 011: 0.5*2us ..... 111:0.5*2^5us
0	R/W	0x0	MOD_EN. Module Enable. 0: Disable 1: Enable

4.3.4.77. PS Counter Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: PS_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	PS_CNT. PS Counter.

4.4. CPU Configuration

4.4.1. Overview

CPU Configuration(CPU CFG) module is used to configure related CPU parameters, including power on, reset, cache, debug, and check the status of CPU. It will be used when you want to disable/enable the CPU, cluster switch, CPU status check, and debug, etc.

Features:

- Software Reset Control for every CPU
- CPU Configuration for every CPU
- One 64-bit common counter

4.4.2. Block Diagram

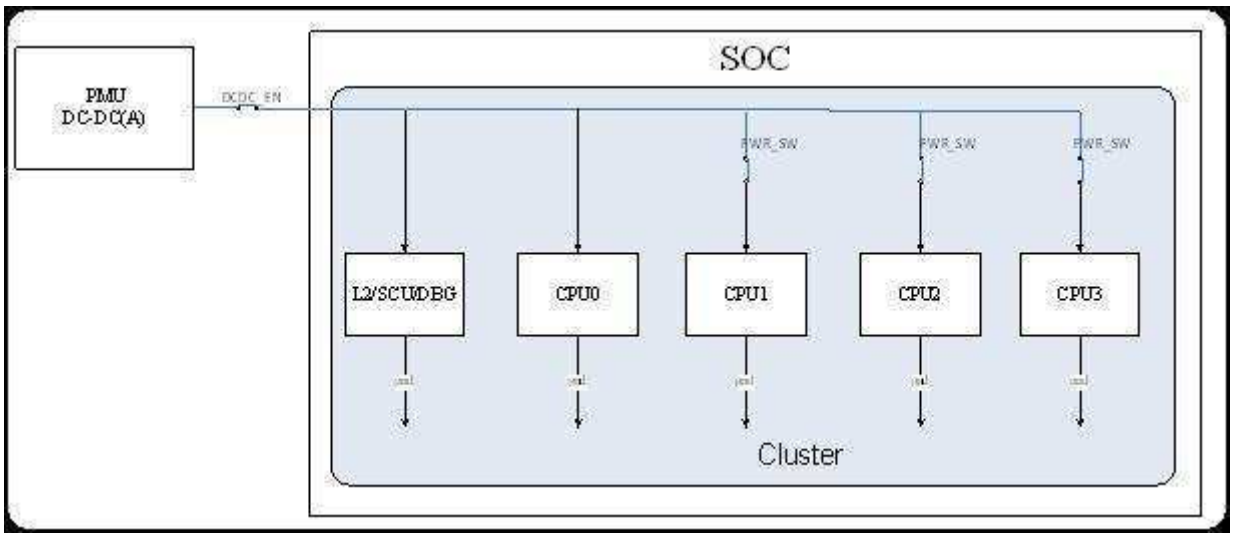


Figure 4-11. CPU CFG Block Diagram

The figure above lists the power domains at CPU reset status. All power switch of CPU core are default to be closed. Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

4.4.3. Operations and Functional Descriptions

4.4.3.1. Signal Description

For the detail of CPU signal, please refer to ***ARM Cortex-A53 TRM***.

4.4.3.2. L2 Idle Mode

When the L2 of Cluster needs to enter WFI mode, firstly make sure the CPU0/1/2/3 of Cluster enter WFI mode, which can be checked through **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing related register bit to 1, and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Remember to set the **ACINACTM** to low when exiting the L2 idle mode.

4.4.3.3. CPU Reset System

The CPU reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**.

4.4.3.4. Operation Principle

The CPU-related operation needs proper configuration of CPUCFG related register, as well as related system control resource including BUS, clock ,reset and power control.

4.4.4. Register List

Module Name	Base Address
CPU CFG	0x01700000

Register Name	Offset	Description
C_CTRL_REG0	0x0000	Cluster Control Register0
C_CTRL_REG1	0x0004	Cluster Control Register1
CACHE_CFG_REG0	0x0008	Cache parameters configuration register0
CACHE_CFG_REG1	0x000C	Cache parameters configuration register1
GENER_CTRL_REG0	0x0028	General Control Register0
C_CPU_STATUS	0x0030	Cluster CPU Status Register
L2_ STATUS_REG	0x003C	L2 Status Register
C_RST_CTRL	0x0080	Cluster Reset Control Register
RVBARADDR0_L	0x00A0	Reset Vector Base Address Register0_L
RVBARADDR0_H	0x00A4	Reset Vector Base Address Register0_H

RVBARADDR1_L	0x00A8	Reset Vector Base Address Register1_L
RVBARADDR1_H	0x00AC	Reset Vector Base Address Register1_H
RVBARADDR2_L	0x00B0	Reset Vector Base Address Register2_L
RVBARADDR2_H	0x00B4	Reset Vector Base Address Register2_H
RVBARADDR3_L	0x00B8	Reset Vector Base Address Register3_L
RVBARADDR3_H	0x00BC	Reset Vector Base Address Register3_H

4.4.5. Register Description

4.4.5.1. Cluster Control Register0 (Default Value: 0x8000_0000)

Offset: 0x0000			Register Name: C_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SYSBAR_DISABLE. Disable broadcasting of barriers onto system bus 0: Barriers are broadcast onto system bus, this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus. This is compatible with an AXI3 interconnect.
30	R/W	0x0	BROADCAST_INNER. Enable broadcasting of Inner Shareable transactions 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.
29	R/W	0x0	BROADCAST_OUTER. Enable broadcasting of outer shareable transactions 0: Outer Shareable transactions are not broadcasted externally. 1: Outer Shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:24	R/W	0x0	AA64nAA32 Register width state. Determines which execution state the processor boots into after a cold reset. 0: AArch32 1: AArch64
23:10	/	/	/

11:8	R/W	0x0	CP15S_DISABLE. Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE. Disable automatic L2 cache invalidate at reset 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3:0	/	/	/

4.4.5.2. Cluster Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: C_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ACINACTM. Snoop interface is inactive and no longer accepting requests. 0: Snoop interface is active 1: Snoop interface is inactive

4.4.5.3. Cache Parameter Control Register0 (Default Value: 0x2222_2222)

Offset: 0x0008			Register Name: CACHE_CFG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x2	L1SDT_DELAY
27	/	/	/
26:24	R/W	0x2	L1TLB_DELAY
23	/	/	/
22:20	R/W	0x2	BTAC_DELAY
19	/	/	/
18:16	R/W	0x2	L1DY_DELAY
15	/	/	/
14:12	R/W	0x2	L1DT_DELAY
11	/	/	/
10:8	R/W	0x2	L1DD_DELAY
7	/	/	/
6:4	R/W	0x2	L1IT_DELAY
3	/	/	/
2:0	R/W	0x2	L1ID_DELAY

4.4.5.4. Cache Parameter Control Register1 (Default Value: 0x0202_2020)

Offset: 0x000C			Register Name: CACHE_CFG_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x2	EMAW
23:19	/	/	/
18:16	R/W	0x2	EMA
15	/	/	/
14:12	R/W	0x2	L2V_DELAY
11:8	/	/	/
7	/	/	/
6:4	R/W	0x2	L2T_DELAY
3:0	/	/	/

4.4.5.5. General Control Register0 (Default Value: 0x0000_0010)

Offset: 0x0028			Register Name: GENER_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state.This bit must remain HIGH for at least one clock cycle to be visible by the cores.
23:20	R/W	0x0	EXM_CLR[3:0]
19:17	/	/	/
16	R/W	0x0	CLREXMONREQ Clearing of the external global exclusive monitor request.When this bit is asserted, it acts as a WFE wake-up event to all the cores in the MPCore device.
15:12	R/W	0x0	CRYPTODISABLE Disable the Cryptography Extensions.
11:9	/	/	/
8	R/W	0x0	L2FLUSHREQ L2 hardware flush request.
7:5	/	/	/
4	R/W	0x1	GICCDISABLE. Globally disables the CPU interface logic and routes the "External" signals directly to the processor: 0: Enable the GIC CPU interface logic. 1: Disable the GIC CPU interface logic.
3:0	/	/	/

4.4.5.6. Cluster CPU Status Register (Default Value: 0x000E_0000)

Offset: 0x30			Register Name: C_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R	0x0	SMP Indicates whether a core is taking part in coherency. 0: Disable 1: Enable
23:20	/	/	/
19:16	R	0xE	STANDBYWFI. Indicates if a core is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:12	/	/	/
11:8	R	0x0	STANDBYWFE. Indicates if a core is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2. Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Active 1: Idle

4.4.5.7. L2 Status Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R	0x0	L2FLUSHDONE L2 hardware flush complete
9	R	0x0	EVENTO Event output. This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8	R	0x0	CLREXMONACK Clearing of the external global exclusive monitor acknowledge.
7:0	/	/	/

4.4.5.8. CPU2 Reset Control Register(Default Value: 0x1110_1101)

Offset: 0x80			Register Name: C_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset. 0: Assert 1: De-assert
27:25	/	/	/
24	R/W	0x1	SOC_DBG_RST. Cluster SOC Debug P_Reset. Clear this bit will reset the SOC Debug Bus Logic and it will automatically change to 1 after 64 p_cycles. 0: Assert 1: De-assert.
23:21	R/W	0x0	
20	R/W	0x1	MBIST_RST CPUBIST Reset. The reset signal for test. 0: Assert 1: De-assert
19:16	R/W	0x0	/
15:13	/	/	/
12	R/W	0x1	HRESET. Cluster H_Reset. Reset all the Cluster Logic and Cluster Interface Logic. 0: Assert 1: De-assert
11:9	/	/	/
8	R/W	0x1	L2_RST. Cluster L2 Cache Reset 0: Assert 1: De-assert
7:4	/	/	/
3:0	R/W	0x1	CORE_RESET. Control a Core Reset Assert. 0: Assert 1: De-assert

4.4.5.9. Reset Vector Base Address Register0_L (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: RVBARADDR0_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU0.
1:0	/	/	/

4.4.5.10. Reset Vector Base Address Register0_H (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: RVBARADDR0_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2]for executing in 64-bit state (AArch64) of CPU0.

4.4.5.11. Reset Vector Base Address Register1_L (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: RVBARADDR1_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU1.
1:0	/	/	/

4.4.5.12. Reset Vector Base Address Register1_H (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: RVBARADDR1_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of CPU1.

4.4.5.13. Reset Vector Base Address Register2_L (Default Value: 0x0000_0000)

Offset: 0x00B0	Register Name: RVBARADDR2_L

Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU2.
1:0	/	/	/

4.4.5.14. Reset Vector Base Address Register2_H (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: RVBARADDR2_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of CPU2.

4.4.5.15. Reset Vector Base Address Register3_L (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: RVBARADDR3_L
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	RVBARDDR[31:2] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64)of CPU3.
1:0	/	/	/

4.4.5.16. Reset Vector Base Address Register3_H (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: RVBARADDR3_H
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	RVBARDDR[39:32] Reset Vector Base Address[39:2] for executing in 64-bit state (AArch64) of CPU3.

4.5. System Control

4.5.1. Overview

Area	Size(Bytes)
SRAM A1	32K
SRAM A2	64K
SRAM C	112K
CPUX I-Cache	32K (X=0,1,2,3)
CPUX D-Cache	32K (X=0,1,2,3)
CPU L2 Cache	512K
Total	976K

4.5.2. Register List

Module Name	Base Address
System Control	0x01C00000

Register Name	Offset	Description
VER_REG	0x24	Version Register
EMAC_EPHY_CLK_REG	0x30	EMAC-EPHY Clock Register

4.5.3. Register Description

4.5.3.1. Version Register (Default Value: UDF)

Offset:0x0024			Register Name: VER_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R	UDF	UBOOT_SEL_PAD_STA. U_boot Select Pin Status. 0: U_Boot 1: Normal Boot
7:0	R	0x0	Reserved

4.5.3.2. EMAC-EPHY Clock Register (Default Value: 0x0005_8000)

Offset:0x0030			Register Name: EMAC_EPHY_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	BPS_EFFUSE
27	R/W	0x0	XMII_SEL 0: Internal SMI and MII 1: External SMI and MII
26:25	R/W	0x0	EPHY_MODE Operation Mode Selection 00: Normal Mode 01: Sim Mode 10: AFE Test Mode 11: /
24:20	R/W	0x0	PHY_ADDR PHY Address
19	R/W	0x0	BIST_CLK_EN 0: BIST clk disable 1: BIST clk enable
18	R/W	0x1	CLK_SEL 0: 25MHz 1: 24MHz
17	R/W	0x0	LED_POL 0: High active 1: Low active
16	R/W	0x1	SHUTDOWN 0: Power up 1: Shutdown
15	R/W	0x1	PHY_SELECT. 0: External PHY 1: Internal PHY
14	/	/	/
13	R/W	0x0	RMII_EN 0: Disable RMII Module 1: Enable RMII Module When this bit assert, MII or RGMII interface is disabled(This means bit13 is

			prior to bit2)
12:10	R/W	0x0	ETXDC. Configure EMAC Transmit Clock Delay Chain.
9:5	R/W	0x0	ERXDC. Configure EMAC Receive Clock Delay Chain.
4	R/W	0x0	ERXIE Enable EMAC Receive Clock Invertor. 0: Disable 1: Enable
3	R/W	0x0	ETXIE Enable EMAC Transmit Clock Invertor. 0: Disable 1: Enable
2	R/W	0x0	EPIT EMAC PHY Interface Type 0: MII 1: RGMII
1:0	R/W	0x0	ETCS. EMAC Transmit Clock Source 00: Transmit clock source for MII 01: External transmit clock source for GMII and RGMII 10: Internal transmit clock source for GMII and RGMII 11: Reserved

4.6. Timer

4.6.1. Overview

Timer 0/1 can take their inputs from Internal OSC(INOSC) or OSC24M. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode. When the current value in **Timer 0 Current Value Register** or **Timer 1 Current Value Register** is counting down to zero, the timer will generate interrupt if the interrupt enable bit is set.

The watchdog is used to resume the controller operation when it is disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds (512000 cycles). It can generate a general reset or interrupt request.

Audio-Video-Sync(AVS) counter is used to synchronize video and audio in the player.

Features:

- 2 Timers for system scheduler counting using OSC24M or INOSC(16MHz) clock
- Each Timer could generate individual interrupt
- 1 Watchdog for resetting whole system or interrupt
- 2 AVS counters for synchronizing video and audio in the player

4.6.2. Block Diagram

The Timer clock comes from one of the two clock sources that could be pre-scaled up to 128 division. In single mode, when **Current Value** counts down to 0 , the enable bit is cleared automatically and Timer stops working. But in continuous mode, **Interval Value** will be auto-reloaded into **Timer 0 Current Value Register**/**Timer 1 Current Value Register** and counter counts from the new interval value again when current value is counted down to 0. Every time current value is counted down to 0, a **Pending** will be generated. **Pending** could be sent to GIC only if **IRQ Enable** bit is set.

Generally watchdog could not count down to 0 because it would be restart inside Interval Value. Otherwise the malfunction makes the watchdog counts down to 0, and pending will be generated, which causes a reset for the whole system or an interrupt (see **Watchdog Configuration Register**).

AVS has two up-counted counters. The clock source of the counter comes from 24MHz/Divisor_N (Divisor_N is set in **AVS Counter Divisor Register**). AVS counter can disable or enable at any time, the Interval Value set in **AVS Counter 0 Register** or **AVS Counter 1 Register** and Divisor Value set in **AVS Counter Divisor Register**. When you enable the AVS counter, it counts up from Interval Value until you pause it. It doesn't generate any pending.

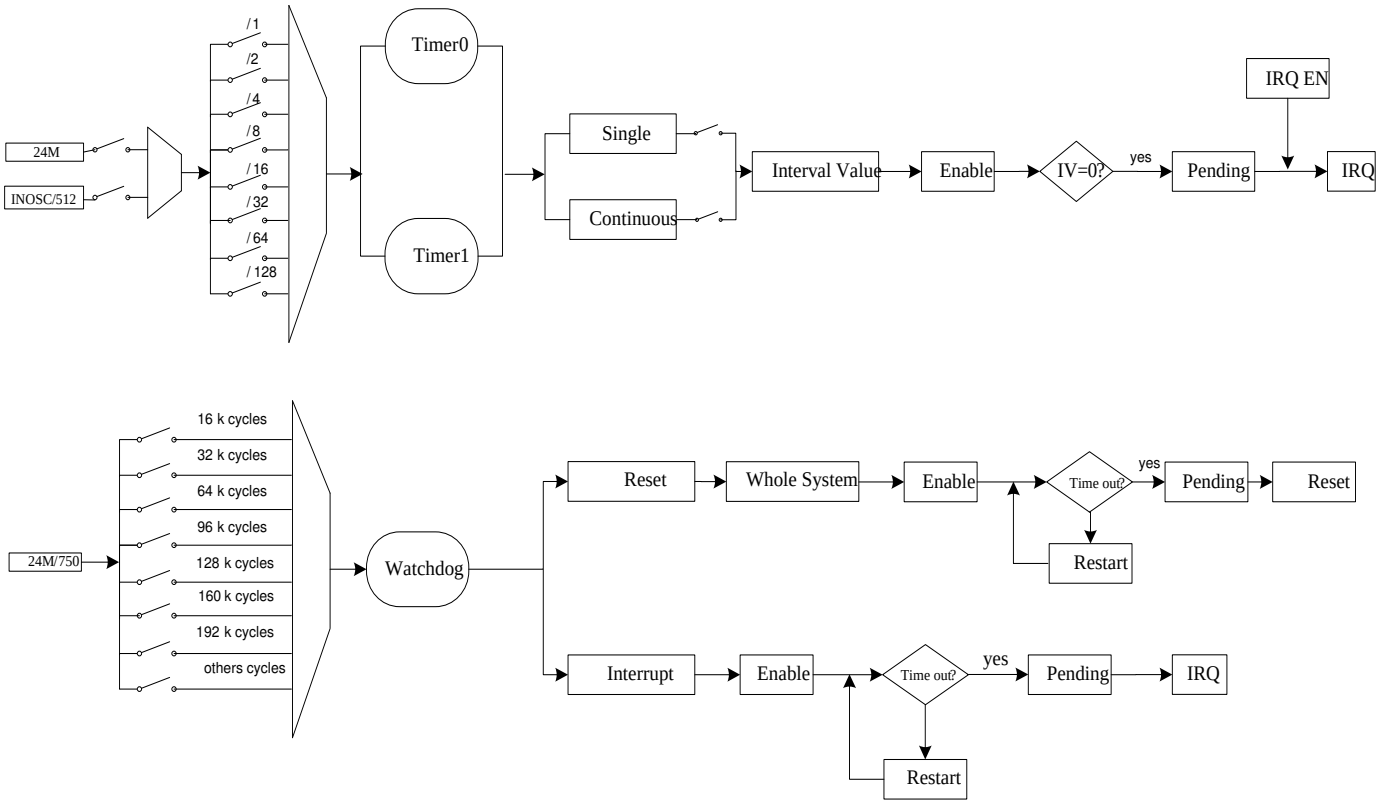


Figure 4-12. Timer Block Diagram

4.6.3. Operations and Functional Descriptions

4.6.3.1. Timer Reload and Enable Bit

Generally the operation of setting both reload bit and enable bit and writing them into **Timer 0 Control Register**/**Timer 1 Control Register** moreover could cause a risk. It had better to enable Timer after Interval Value is loaded into **Timer 0 Current Value Register**/**Timer 1 Current Value Register**. Only in timer pause time, when you hope that counter starts working from a new interval value, the reload bit and enable bit should be set 1 and wrote into **TMR0_CTRL_REG**/ **TMR1_CTRL_REG** at the same time.

4.6.3.2. Timing Requirement for Timer Command

For reload and enable operation of Timer, it is necessary to wait some cycles between the same continuous operations. It has to wait for 2 cycles at least from pause state to start or from start state to pause. To reload operation, it could not be implemented immediately again until the reload bit is cleared automatically the last operation.

4.6.3.3. Watchdog Restart

Watchdog restart function should be enabled inside Interval Value. Make a restart by writing 1 to **Watchdog Restart** and 0xA57 to **Watchdog Key Field** at the same time .

4.6.3.4. Programming Guide

(1) Timer

Take making a Timer0 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR0_INTV_VALUE_REG);                          //Set interval value
writel(0x94, TMR0_CTRL_REG);                                 //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR0_CTRL_REG)|(1<<1), TMR0_CTRL_REG); //Set Reload bit
while((readl(TMR0_CTRL_REG)>>1)&1);                          //Waiting Reload bit turns to 0
writel(readl(TMR0_CTRL_REG)|(1<<0), TMR0_CTRL_REG); //Enable Timer0
```

(2) Watchdog Reset

In the following instance making configurations for Watchdog: configurate clock source as 24M/750, configurate Interval value as 1s and configurate watchdog Configuration as **To whole system**. This instance indicates that reset system after 1s.

```
writel(0x1, WDOG0_CFG_REG);                                  //To whole system
writel(0x10, WDOG0_MODE_REG);                                //Interval Value set 1s
writel(readl(WDOG0_MODE_REG)|(1<<0), WDOG0_MODE_REG);      //Enable Watchdog
```

(3) Watchdog Restart

In the following instance making configurations for Watchdog: configurate clock source as 24M/750, configurate Interval Value as 1s and configurate Watchdog Configuration as **To whole system**. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(0x1, WDOG0_CFG_REG);                                  //To whole system
writel(0x10, WDOG0_MODE_REG);                                //Interval Value set 1s
writel(readl(WDOG0_MODE_REG)|(1<<0), WDOG0_MODE_REG);      //Enable Watchdog
----other codes---
writel(readl(WDOG0_CTRL_REG)|(0xA57<<1)|(1<<0), WDOG0_CTRL_REG); //Writel 0xA57 at Key Field and Restart Watchdog
```


4.6.4. Register List

Module Name	Base Address
TIMER	0x01C20C00

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
AVS_CNT_CTL_REG	0x0080	AVS Control Register
AVS_CNT0_REG	0x0084	AVS Counter 0 Register
AVS_CNT1_REG	0x0088	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x008C	AVS Divisor Register
WDOG0_IRQ_EN_REG	0x00A0	Watchdog 0 IRQ Enable Register
WDOG0_IRQ_STA_REG	0x00A4	Watchdog 0 Status Register
WDOG0_CTRL_REG	0x00B0	Watchdog 0 Control Register
WDOG0_CFG_REG	0x00B4	Watchdog 0 Configuration Register
WDOG0_MODE_REG	0x00B8	Watchdog 0 Mode Register

4.6.5. Register Description

4.6.5.1. Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect. 1: Timer 1 interval value reached interrupt enable.
0	R/W1S	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect. 1: Timer 0 interval value reached interrupt enable.

4.6.5.2. Timer IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect. 1: Pending, timer 1 interval value is reached.
0	R/W1C	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect. 1: Pending, timer 0 interval value is reached.

4.6.5.3. Timer 0 Control Register (Default Value: 0x0000_0004)

Offset:0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer 0 Clock Source.

			00: Internal OSC / N 01: OSC24M. 10: / 11: / Internal OSC / N is about 32KHz.
1	R/W1S	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value. After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause 1: Start. When the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the **TMR0_EN** bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the **TMR0_EN** bit can be set to 1. In timer pause state,**Timer 0 Interval Value Register** can be modified. If the timer is started again, and the software hope **Timer 0 Current Value Register** to down-count from the new interval value, the **Timer 0 Reload** bit and the **Timer 0 Enable** bit should be set to 1 at the same time.

4.6.5.4. Timer 0 Interval Value Register (Default Value: 0x0000_0000)

Offset:0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE. Timer 0 Interval Value.

Note: The value should consider the system clock and the timer clock source.

4.6.5.5. Timer 0 Current Value Register (Default Value: 0x0000_0000)

Offset:0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE.

			Timer 0 Current Value.

Note: Timer0 current value is a 32-bit down-counter (from interval value to 0).

4.6.5.6. Timer 1 Control Register (Default Value: 0x0000_0004)

Offset:0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. 00: Internal OSC / N 01: OSC24M. 10: / 11: /. Internal OSC / N is about 32KHz.
1	R/W1S	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR1_EN. Timer 1 Enable.

			0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the **TMR1_EN** bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the **TMR1_EN** bit can be set to 1. In timer pause state, **Timer 1 Interval Value Register** can be modified. If the timer is started again, and the software hope **Timer 1 Current Value Register** to down-count from the new interval value, the **Timer 1 Reload** bit and the **Timer 1 Enable** bit should be set to 1 at the same time.

4.6.5.7. Timer 1 Interval Value Register (Default Value: 0x0000_0000)

Offset:0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value.

Note: The value setting should consider the system clock and the timer clock source.

4.6.5.8. Timer 1 Current Value Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: TMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

Note: The current value of Timer1 is a 32-bit down-counter (from interval value to 0).

4.6.5.9. AVS Counter Control Register (Default Value: 0x0000_0000)

Offset:0x0080			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS. Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1.
8	R/W	0x0	AVS_CNT0_PS. Audio/Video Sync Counter 0 Pause Control

			0: Not pause 1: Pause Counter 0.
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable.
0	R/W	0x0	AVS_CNT0_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable.

4.6.5.10. AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset:0x0084			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0. Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33 bits counter register. The initial value of the internal 33 bits counter register can be set by software. The LSB bit of the 33 bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting **AVS_CNT0_PS** to '1'. When it is paused, the counter will not increase.

4.6.5.11. AVS Counter 1 Register (Default Value: 0x0000_0000)

Offset:0x0088			Register Name: AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1. Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33 bits counter register. The initial value of the internal 33 bits counter register can be set by software. The LSB bit of the 33 bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting **AVS_CNT1_PS** to '1'. When it is paused, the counter will not increase.

4.6.5.12. AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset:0x008C			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D. Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33 bits counter engine will maintain another 12 bits counter. The 12 bits counter is used for counting the cycle number of one 24MHz clock. When the 12 bits counter reaches (>= N) the divisor value, the internal 33 bits counter register will increase 1 and the 12 bits counter will reset to zero and restart again.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D. Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33 bits counter engine will maintain another 12 bits counter. The 12 bits counter is used for counting the cycle number of one 24MHz clock. When the 12 bits counter reaches (>= N) the divisor value, the internal 33 bits counter register will increase 1 and the 12 bits counter will reset to zero and restart again.

Note: **AVS_CNT1_D** and **AVS_CNT0_D** can be configured by software at any time.

4.6.5.13. Watchdog0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x00A0			Register Name: WDOG0_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG0_IRQ_EN. Watchdog0 Interrupt Enable. 0: No effect. 1: Watchdog0 interrupt enable.

4.6.5.14. Watchdog0 Status Register (Default Value: 0x0000_0000)

Offset:0x00A4			Register Name: WDOG0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	WDOG0_IRQ_PEND. Watchdog0 n IRQ Pending. Setting 1 to the bit will clear it. 0: No effect. 1: Pending. Watchdog0 interval value is reached.

4.6.5.15. Watchdog0 Control Register (Default Value: 0x0000_0000)

Offset:0x00B0			Register Name: WDOG0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	WDOG0_KEY_FIELD. Watchdog0 Key Field. Should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG0_RSTART. Watchdog0 Restart. 0: No effect. 1: Restart watchdog0.

4.6.5.16. Watchdog0 Configuration Register (Default Value: 0x0000_0001)

Offset:0x00B4			Register Name: WDOG0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	WDOG0_CONFIG. Watchdog0 generates a reset signal 00: / 01: To whole system 10: Only interrupt 11: /

4.6.5.17. Watchdog0 Mode Register (Default Value: 0x0000_0000)

Offset:0x00B8			Register Name: WDOG0_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG0_INTV_VALUE. Watchdog0 Interval Value Watchdog0 clock source is *OSC24M / 750*. If the clock source is turned off, Watchdog 0 will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) others: /
3:1	/	/	/
0	R/W1S	0x0	WDOG0_EN. Watchdog0 Enable. 0: No effect 1: Enable watchdog0.

4.7. Trusted Watchdog

4.7.1. Overview

The trusted watchdog(TWD) is primarily used to protect the trusted world operations from denial of service when secure services are dependent to the RichOS scheduler. For example, if the trusted world is not entered after a defined time limit, the SoC is re-started to perform an authentication of the system.

The trusted watchdog can also be used to mask the real cause of a security error thanks to the delayed warm reset it generates.

4.7.2. Block Diagram

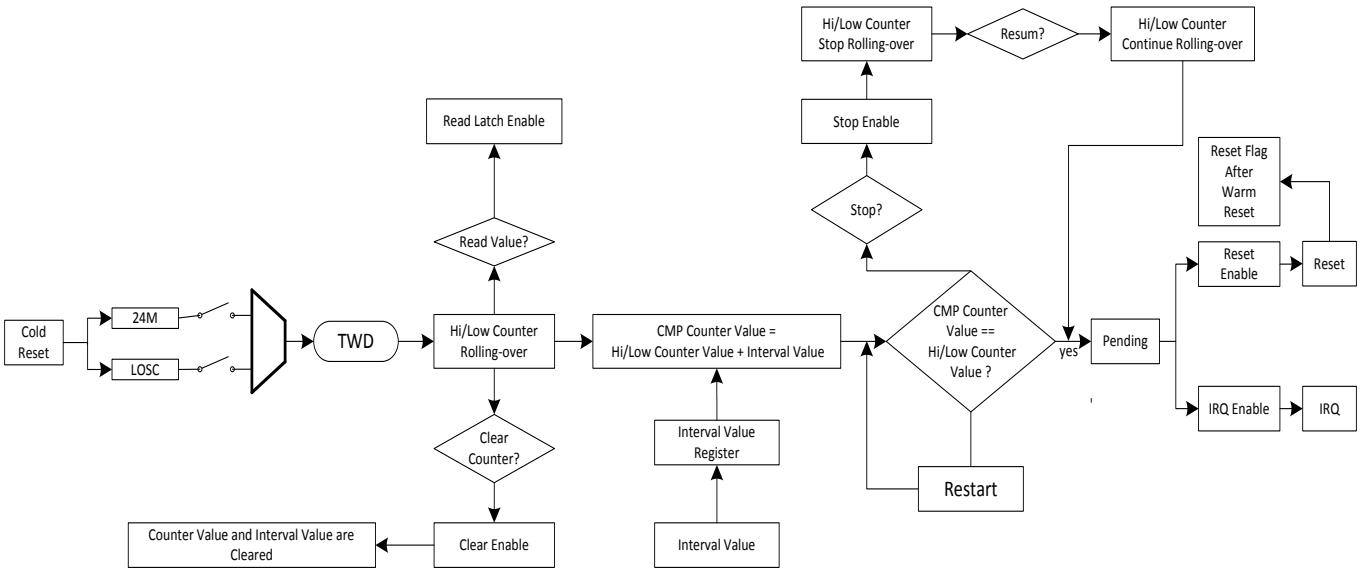


Figure 4-13. TWD Block Diagram

The trusted watchdog timer must always run when the SoC wakes up from cold reset and can be refreshed, suspended, or reset only by secure accesses. And a clock of at least 32 KHz is used when the device is not a power saving cycles.

4.7.3. Operations and Functional Descriptions

4.7.3.1. TWD Reset

The trusted watchdog timer is able to generate a SoC warm reset after a duration programmed into the timer or set by

default in hardware. And the flag indicating the occurrence of a watchdog triggered warm reset has occurred since the last cold reset.

Clock sources driving the watchdog timer must be controlled or managed by a trusted entity. This means that non-trusted world accesses are not permitted to turn on, turn off or modify the characteristics of clock source. The ***Clear Enable*** will reset relevant bits in the watchdog registers, except the reset flag.

4.7.3.2. NV-Counter

After a firmware image is validated, the image revision number taken from the certificate extension field, for example, ***Trusted Firmware NV-Counter*** is compared with the corresponding NV-Counter stored in hardware. If the value is:

- Less than the associated NV-Counter, then the authentication fail.
- Identical to the NV-Counter, then the authentication is successful.
- More than the NV-Counter, then the authentication are successful and the NV-Counter is updated.

The 2^32 monotonic counter does not need to be e-Fuses, but it does need to be fully secure. Using the SoC embedded NVM, or external secure element, or a trusted register, which is always on power.

The **Secure Storage NV-Counter Register** is used for protecting the trusted world Secure Storage (SST) file from replay attacks, since SST contains subsidiary relay attacks protection counters for each Trusted Application.

Four 32-bit counters are used for counting 2^32 states for synchronizing data stores against replay attacks. These counters are optionally required since they can be handled by a Trusted OS service using the secure storage at boot time or using eMMC Replay Protected Memory Block (RPMB).

4.7.4. Register List

Module Name	Base Address
TWD	0x01F01800

Register Name	Offset	Description
TWD_STATUS_REG	0x0000	TWD Status Register
TWD_CTRL_REG	0x0010	TWD Control Register
TWD_RESTART_REG	0x0014	TWD Restart Register
TWD_LOW_CNT_REG	0x0020	TWD Low Counter Register
TWD_HIGH_CNT_REG	0x0024	TWD High Counter Register
TWD_INTV_VAL_REG	0x0030	TWD Interval Value Register
TWD_LOW_CNT_CMP_REG	0x0040	TWD Low Counter Compare Register
TWD_HIGH_CNT_CMP_REG	0x0044	TWD High Counter Compare Register
SST_NV_CNT_REG	0x0100	Secure Storage NV-Counter Register
SYN_DATA_CNT_REG0	0x0110	Synchronize Data Counter Register 0
SYN_DATA_CNT_REG1	0x0114	Synchronize Data Counter Register 1

SYN_DATA_CNT_REG2	0x0118	Synchronize Data Counter Register 2
SYN_DATA_CNT_REG3	0x011C	Synchronize Data Counter Register 3

4.7.5. Register Description

4.7.5.1. TWD Status Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWD_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	TWD_PEND_FLAG. Interrupt pending. Setting 1 to the bit will clear it. 0: No effect. 1: Pending.

4.7.5.2. TWD Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: TWD_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit counter clock source select. 0: LOSC. 1: OSC24M.
30:10	/	/	/
9	R/W	0x0	TWD_RESET_EN. TWD reset enable. 0: Reset disable. 1: Reset enable.
8	R/W	0x0	TWD_INT_EN. TWD Interrupt Enable. 0: Interrupt disable. 1: Interrupt enable.
7:2	/	/	/
1	R/W	0x0	TWD_STOP_EN. TWD stop enable. 0: Resume rolling-over.

			1: Stop rolling-over.
0	R/W	0x0	TWD_CLR_EN. TWD clear enable. 0: No effect. 1: To clear relevant registers, it will change to zero after the registers are cleared.

4.7.5.3. TWD Restart Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TWD_RESTART_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	W	0x0	TWD_RESTART_KEYFILED. It should be written to 0xD14. Writing any other value in this field aborts the write operation.
15:1	/	/	/
0	W	0x0	TWD_RESTART_EN. If writing '1' to this bit, the value of *Counter Compare Registers* would change. 0: No effect. 1: Restart enable.

4.7.5.4. TWD Low Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TWD_LOW_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TWD_LOW_CNT. The TWD low 32-bit counter.

4.7.5.5. TWD High Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TWD_HIGH_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TWD_HIGH_CNT. The TWD high 32-bit counter.

4.7.5.6. TWD Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0030	Register Name: TWD_INTV_VAL_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TWD_INTV_VAL. The TWD interval value.

4.7.5.7. TWD Low Counter Compare Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TWD_LOW_CNT_CMP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TWD_LOW_CMP. The TWD low 32-bit compare counter.

4.7.5.8. TWD High Counter Compare Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: TWD_HIGH_CNT_CMP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TWD_HIGH_CMP. The TWD high 32-bit compare counter.

4.7.5.9. Secure Storage NV-Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SST_NV_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SST_NV_CNT. This counter protects the trusted world secure storage file from replay attacks.

4.7.5.10. Synchronize Data Counter Register 0 (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: SYN_DATA_CNT_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SYN_DATA_CNT0. This counter is used for synchronizing data stores against replay attacks.

4.7.5.11. Synchronize Data Counter Register 1 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: SYN_DATA_CNT_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SYN_DATA_CNT1. This counter is used for synchronizing data stores against replay attacks.

4.7.5.12. Synchronize Data Counter Register 2 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: SYN_DATA_CNT_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SYN_DATA_CNT2. This counter is used for synchronizing data stores against replay attacks.

4.7.5.13. Synchronize Data Counter Register 3 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SYN_DATA_CNT_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SYN_DATA_CNT3. This counter is used for synchronizing data stores against replay attacks.

4.8. RTC

4.8.1. Overview

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator and an independent power pin (RTC-VIO).

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated. In this section, there are two kinds of alarm. Alarm 0 is a general alarm, its counter is based on second. Alarm 1 is a weekly alarm, its counter is based on the real time.

The 32768Hz oscillator is used only to provide a low power, accurate reference for the RTC.

4.8.2. Register List

Module Name	Base Address
RTC	0x01F00000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
RTC_YY_MM_DD_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM-SS	0x0040	Alarm 1 Week HMS Register
ALARM1_ENABLE_REG	0x0044	Alarm 1 Enable Register
ALARM1_IRQ_EN	0x0048	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	0x004C	Alarm 1 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
LOSC_OUT_GATING_REG	0x0060	LOSC Output Gating Register
GP_DATA_REG	0x0100 + N*0x0004	General Purpose Register (N=0~7)
GPL_HOLD_OUTPUT_REG	0x0180	GPL Hold Output Register

RTC-VIO_REG	0x0190	RTC-VIO Regulate Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
CRY_CONFIG_REG	0x0210	Crypto Configuration Register
CRY_KEY_REG	0x0214	Crypto Key Register
CRY_EN_REG	0x0218	Crypto Enable Register

4.8.3. Register Description

4.8.3.1. LOSC Control Register (Default Value: 0x0000_4000)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN. LOSC auto switch enable. 0: Disable 1: Enable.
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE. ALARM DD-HH-MM-SS access. After writing the **Alarm 1 Week HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After writing the **RTC HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished. After writing the **RTC HH-MM-SS Register**, the **RTC HH-MM-SS Register** will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the **RTC YY-MM-DD Register**, this bit is set and it will be cleared until the real writing operation is finished. After writing the **RTC YY-MM-DD Register**, the **RTC YY-MM-DD Register** will be refreshed for at most one second.
6:4	/	/	/
3:2	R/W	0x0	EXT_LOSC_GSM. External 32768Hz Crystal GSM.

			00: Low 01: / 10: / 11 High
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL. LOSC Clock source Select. '**N**' is the value of **Internal OSC Clock Prescalar Register**. 0: InternalOSC /32/ N 1: External 32.768kHz OSC. (InternalOSC = 16MHz)

Note: If the bit[9:7] of **LOSC_CTRL_REG** is set, the corresponding of **Alarm 1 Week HH-MM-SS Register**, **RTC HH-MM-SS Register**, **RTC YY-MM-DD Register** can't be written.

4.8.3.2. LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			**Register Name: LOSC_AUTO_SWT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND. LOSC auto switch pending. 0: No effect 1: Auto switches pending Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. '**N**' is the value of **Internal OSC Clock Prescalar Register**. 0: InternalOSC /32/ N 1: External 32.768KHz OSC (InternalOSC = 16MHz)

4.8.3.3. Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			**Register Name: INTOSC_CLK_PRESCAL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF	INTOSC_CLK_PRESCAL.

			Internal OSC Clock Prescalar value N. 0x000: 1 0x001: 2 0x002: 3 ..... 0x1F: 32

4.8.3.4. RTC YY-MM-DD Register (Default Value: UDF)

Offset:0x0010			Register Name: RTC_YY_MM_DD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	LEAP. Leap Year. 0: Not 1: Leap year. This bit can not set by hardware. It should be set or cleared by software.
21:16	R/W	UDF	YEAR. Year. Range from 0~63.
15:12	/	/	/
11:8	R/W	UDF	MONTH. Month. Range from 1~12.
7:5	/	/	/
4:0	R/W	UDF	DAY. Day. Range from 1~31.

Note: If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area.

The number of days in different month may be different.

4.8.3.5. RTC HH-MM-SS Register (Default Value: UDF)

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	WK_NO. Week number. 000: Monday

			001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
28:21	/	/	/
20:16	R/W	UDF	HOUR. Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND. Range from 0~59

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

4.8.3.6. Alarm 0 Counter Register (Default Value: 0x0000_0000)

Offset:0x0020			**Register Name: ALARM0_COUNTER_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	ALARM0_COUNTER. Alarm 0 Counter is based on second.

Note: If the second is set to 0, it will be 1 second in fact.

4.8.3.7. Alarm 0 Current Value Register (Default Value: UDF)

Offset:0x0024			**Register Name: ALARM0_CUR_VLU_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	x	ALARM0_CUR_VLU. Check Alarm 0 Counter Current Values.

Note: If the second is set to 0, it will be 1 second in fact.

4.8.3.8. Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			**Register Name: ALARM0_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. If this bit is set to "1", the valid bits of **Alarm 0 Counter Register** will down count to zero, and the alarm pending bit will be set to "1". 0: Disable 1: Enable

4.8.3.9. Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN. Alarm 0 IRQ Enable. 0: Disable 1: Enable

4.8.3.10. Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND. Alarm 0 IRQ Pending bit. 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

4.8.3.11. Alarm 1 Week HH-MM-SS Register (Default Value: UDF)

Offset:0x0040			Register Name: ALARM1_WK_HH_MM_SS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR. Range from 0~23.
15:14	/	/	/

13:8	R/W	UDF	MINUTE. Range from 0~59.
7:6	/	/	/
5:0	R/W	UDF	SECOND. Range from 0~59.

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

4.8.3.12. Alarm 1 Enable Register (Default Value: 0x0000_0000)

Offset:0x0044			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	WK6_ALM1_EN. Week 6 (Sunday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 6, the week 6 alarm irq pending bit will be set to "1".
5	R/W	0x0	WK5_ALM1_EN. Week 5 (Saturday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 5, the week 5 alarm irq pending bit will be set to "1".
4	R/W	0x0	WK4_ALM1_EN. Week 4 (Friday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the register bit[31:29] of **RTC HH-MM-SS Register** is 4, the week 4 alarm irq pending bit will be set to "1".

3	R/W	0x0	WK3_ALM1_EN. Week 3 (Thursday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 3, the week 3 alarm irq pending bit will be set to "1".
2	R/W	0x0	WK2_ALM1_EN. Week 2 (Wednesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 2, the week 2 alarm irq pending bit will be set to "1".
1	R/W	0x0	WK1_ALM1_EN. Week 1 (Tuesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 1, the week 1 alarm irq pending bit will be set to "1".
0	R/W	0x0	WK0_ALM1_EN. Week 0 (Monday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 0, the week 0 alarm irq pending bit will be set to "1".

4.8.3.13. Alarm 1 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0048	Register Name: ALARM1_IRQ_EN

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN. Alarm 1 IRQ Enable. 0: Disable 1: Enable

4.8.3.14. Alarm 1 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x004C			Register Name: ALARM1_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect 1: Pending, week counter value is reached If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

4.8.3.15. Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

4.8.3.16. LOSC Output Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: LOSC_OUT_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	LOSC_OUT_GATING. Configuration of LOSC output, and without LOSC output by default. 0: Enable LOSC output gating

			1: Disable LOSC output gating

4.8.3.17. General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~7)			Register Name: GP_DATA_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	GP_DATA. Data [31:0].

Note: General purpose register 0~7 value can be stored if the RTC-VIO is larger than 1.0V.

4.8.3.18. GPL Hold Output Register (Default Value: 0x0000_0000)

Offset:0x0180			Register Name: GPL_HOLD_OUTPUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	GPL11_HOLD_OUTPUT. Hold the output of GPIOL11 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
10	R/W	0x0	GPL10_HOLD_OUTPUT. Hold the output of GPIOL10 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
9	R/W	0x0	GPL9_HOLD_OUTPUT. Hold the output of GPIOL9 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
8	R/W	0x0	GPL8_HOLD_OUTPUT. Hold the output of GPIOL8 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable

			1: Hold enable
7	R/W	0x0	GPL7_HOLD_OUTPUT. Hold the output of GPIOL7 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPL6_HOLD_OUTPUT. Hold the output of GPIOL6 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPL5_HOLD_OUTPUT. Hold the output of GPIOL5 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPL4_HOLD_OUTPUT. Hold the output of GPIOL4 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other output may not hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPL3_HOLD_OUTPUT. Hold the output of GPIOL3 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPL2_HOLD_OUTPUT. Hold the output of GPIOL2 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPL1_HOLD_OUTPUT. Hold the output of GPIOL1 when the power of system is changing. The

			output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPL0_HOLD_OUTPUT. Hold the output of GPIOL0 when the power of system is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

4.8.3.19. RTC-VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name: RTC-VIO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x4	RTC-VIO_REGU. These bits are useful for regulating the RTC-VIO from 0.776V to 1.535V. 000: 0.235 * VCC-RTC (0.776V) 001: 0.265 * VCC-RTC (0.8745V) 010: 0.3 * VCC-RTC (0.99V) 011: 0.335 * VCC-RTC (1.1055V) 100: 0.365 * VCC-RTC (1.205V) 101: 0.4 * VCC-RTC (1.32V) 110: 0.435 * VCC-RTC (1.4355V) 111: 0.465 * VCC-RTC (1.535V) **Note:** VCC-RTC = 3.3V

4.8.3.20. IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0			Register Name: IC_CHARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	IC_CHARA. Key Field. The field should be written to 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA. Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

4.8.3.21. Crypto Configuration Register (Default Value: 0x0000_0000)

Offset:0x0210			Register Name: CRY_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field

4.8.3.22. Crypto Key Register (Default Value: 0x0000_0000)

Offset:0x0214			Register Name: CRY_KEY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CRY_KEY Crypto Key

4.8.3.23. Crypto Enable Register (Default Value: 0x0000_0000)

Offset:0x0218			Register Name: CRY_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypto Enable

4.9. High Speed Timer

4.9.1. Overview

The clock sources of High Speed Timer(HSTimer) are fixed to AHBCLK, which is much higher than OSC24M. Compared with other timers, the clock source of HSTimer is synchronized with AHB clock, and when the bit[31] in the **HSTimer Control Register** is set 1, timer goes into the test mode, which is used to system simulation. When the current value in both **HSTimer Current Value Lo Register** and **HSTimer Current Value Hi Register** are counting down to zero, the timer will generate interrupt if the **HS_TMR_INT_EN** bit is set.

Features:

- 1 HSTimer with individual 56-bit counter
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register
- Clock source is synchronized with AHB clock, which means calculating much more accurate than other timers

4.9.2. Operations and Functional Descriptions

4.9.2.1. HSTimer Function Structure

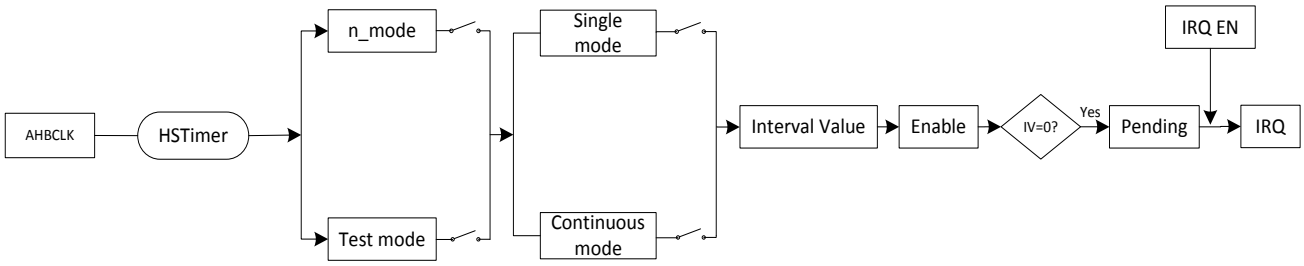


Figure 4-14. HSTimer Function Structure and Work Flow

HSTimer has two work modes. n_mode is used for normal counting and Test mode is used in system simulation. Each work mode has the two count modes: Single mode and Continuous mode. When Current Value counts down to 0, HSTimer will be disabled in Single mode , but HSTimer will not be disabled and counts from Interval value again in Continuous mode. About HSTimer 56-bit counter, it is combined with a low 24-bit counter(**HSTimer Current Value Lo Register**) and a high 32-bit counter(**HSTimer Current Value Hi Register**).

4.9.2.2. HSTimer Clock Gating and Software Reset

By default the clock gating of HSTimer is mask. When it is necessary to use HSTimer, its clock gating should be opened

in the **Bus Clock Gating Register0** and then de-assert the software reset in the **Bus Software Reset Register 0** on CCU module. If it is no need to use HSTimer, both the gating bit and software reset bit should be set 0.

4.9.2.3. HSTimer Reloading Bit

Differing from the reloading of Timer, when the interval value is reloaded into the current value register, the reload bit would not turn to 0 automatically until you clear it. If software hopes the current value register to down-count from the new interval value in pause status, the reload bit and the enable bit should be written 1 at the same time.

4.9.3. Programming Guidelines

Take making a 1us delay using HSTimer for an instance as follow, AHB1CLK will be configurated as 100MHz and n_mode, Single mode and 2 pre-scale will be selected in this instance.

```
writel(0x0, HS_TMR_INTV_VALUE_HI);                          //Set interval value Hi 0x0
writel(0x32, HS_TMR_INTV_VALUE_LO);                         //Set interval value Lo 0x32
writel(0x90, HS_TMR_CTRL_REG);                              //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR_CTRL_REG)|(1<<1), HS_TMR_CTRL_REG);     //Set Reload bit
writel(readl(HS_TMR_CTRL_REG)|(1<<0), HS_TMR_CTRL_REG);     //Enable HSTimer
While(!(readl(HS_TMR_IRQ_STAS_REG)&1));                     //Wait for HSTimer to generate pending
Writel(1,HS_TMR_IRQ_STAS_REG);                              //Clear HSTimer pending
```

4.9.4. Register List

Module Name	Base Address
High Speed Timer	0x01C60000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HSTimer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HSTimer Status Register
HS_TMR_CTRL_REG	0x0010	HSTimer Control Register
HS_TMR_INTV_LO_REG	0x0014	HSTimer Interval Value Low Register
HS_TMR_INTV_HI_REG	0x0018	HSTimer Interval Value High Register
HS_TMR_CURNT_LO_REG	0x001C	HSTimer Current Value Low Register
HS_TMR_CURNT_HI_REG	0x0020	HSTimer Current Value High Register

4.9.5. Register Description

4.9.5.1. HSTimer IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1S	0x0	HS_TMR_INT_EN. High Speed Timer Interrupt Enable. 0: No effect 1: High Speed Timer Interval Value reached interrupt enable.

4.9.5.2. HSTimer IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	HS_TMR_IRQ_PEND. High Speed Timer IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending. High Speed Timer Interval Value is reached.

4.9.5.3. HSTimer Control Register (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: HS_TMR_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR_TEST. High Speed Timer test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode.
30:8	/	/	/
7	R/W	0x0	HS_TMR_MODE. High Speed Timer mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.

6:4	R/W	0x0	HS_TMR_CLK Select the pre-scale of the High Speed Timer clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR_RELOAD. High Speed Timer reload. 0: No effect 1: Reload High Speed Timer Interval Value.
0	R/W	0x0	HS_TMR_EN. High Speed Timer enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

4.9.5.4. HSTimer Interval Value Lo Register (Default Value: UDF)

Offset:0x0014			**Register Name: HS_TMR_INTV_LO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	HS_TMR_INTV_VALUE_LO. High Speed Timer Interval Value [31:0].

4.9.5.5. HSTimer Interval Value Hi Register (Default Value: UDF)

Offset:0x0018	**Register Name: HS_TMR_INTV_HI_REG**

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	UDF	HS_TMR_INTV_VALUE_HI. High Speed Timer Interval Value [55:32].

Note: The interval value register is a 56-bit register. When reading or writing the interval value, the **HSTimer Interval Value Lo Register** should be read or written firstly, the **HSTimer Interval Value Hi Register** should be written after the **HSTimer Interval Value Lo Register**.

4.9.5.6. HSTimer Current Value Lo Register (Default Value: UDF)

Offset:0x001C			Register Name: HS_TMR_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	HS_TMR_CUR_VALUE_LO. High Speed Timer Current Value [31:0].

4.9.5.7. HSTimer Current Value Hi Register (Default Value: UDF)

Offset:0x0020			Register Name: HS_TMR_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	UDF	HS_TMR_CUR_VALUE_HI. High Speed Timer Current Value [55:32].

Note: HSTimer current value is a 56-bit down-counter (from interval value to 0).When reading or writing the current value, the **HSTimer Current Value Lo Register** should be read or written firstly.

4.10. PWM

4.10.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the **PWM Channel Period Register**, PWM resets. At the beginning of a count period cycle, the PWM is set to active state and count from 0x0000.The PWM divider divides the clock(24MHz) by 1~4096 according to the pre-scalar bits in the **PWM Control Register**.

In PWM cycle mode, the output will be a square waveform, the frequency is set in the **PWM Channel Period Register**. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

4.10.2. Block Diagram

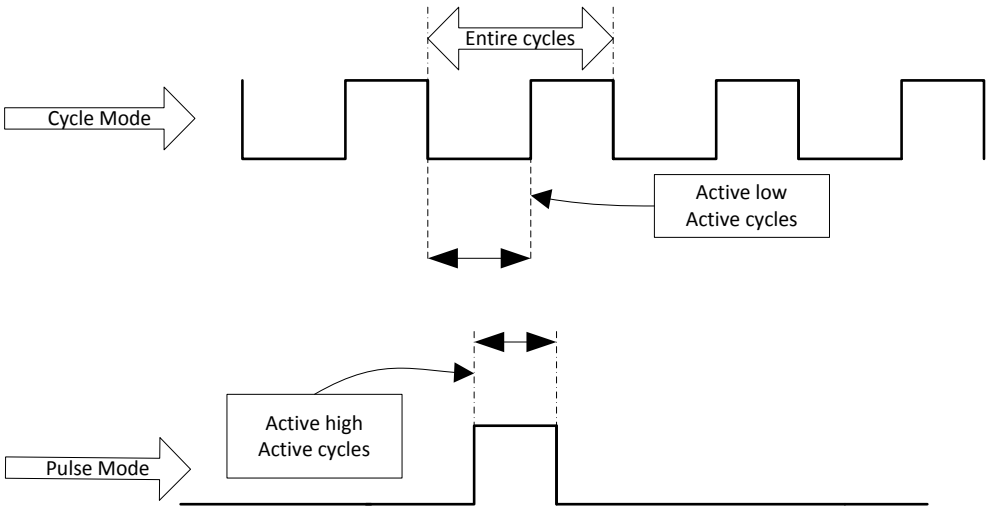


Figure 4-15. PWM Block Diagram

The PWM divider divides the clock (24MHz) by 1-64 according to the pre-scalar bits in the PWM control register. The PWM output frequency can be divided by 65536 at most. In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

4.10.3. Register List

Module Name	Base Address
PWM	0x01C21400

Register Name	Offset	Description
PWM_CH_CTRL	0x0000	PWM Control Register
PWM_CH_PERIOD	0x0004	PWM Channel Period Register

4.10.4. Register Description

4.10.4.1. PWM Control Register(Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PWM_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x0	PWM0_RDY. PWM0 Period Register Ready. 0: PWM0 period register is ready to write 1: PWM0 period register is busy.
27:10	/	/	/
9	R/W	0x0	PWM0_BYPASS. PWM CH0 Bypass Enable. If the bit is set to 1, PWM0 output is OSC24MHz. 0: Disable 1: Enable
8	R/W	0x0	PWM_CH0_PUL_START. PWM Channel 0 Pulse Output Start. 0: No effect 1: Output 1 pulse. The pulse width should be set by the bit[15:0] of **PWM Channel Period Register**,and the pulse state should be set by **PWM Channel 0 Active State**. After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL0_MODE. 0: Cycle mode 1: Pulse mode.
6	R/W	0x0	SCLK_CH0_GATING. Gating the Special Clock for PWM0 0: Mask 1: Pass
5	R/W	0x0	PWM_CH0_ACT_STA.

			PWM Channel 0 Active State. 0: Low Level 1: High Level.
4	R/W	0x0	PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable 1: Enable.
3:0	R/W	0x0	PWM_CH0_PRESCAL. PWM Channel 0 Prescalar. These bits should be set before the PWM Channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1

4.10.4.2. PWM Channel Period Register (Default Value: UDF)

Offset:0x0004			**Register Name: PWM_CH_PERIOD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	PWM_CH0_ENTIRE_CYS Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK (PWM CLK = 24MHz/pre-scale).

15:0	R/W	UDF	PWM_CH0_ENTIRE_ACT_CYS Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Note: The active cycles should be no larger than the period cycles.

4.11. DMA

4.11.1. Overview

The DMA enables data transfers between peripheral I/O devices and memories without using the CPU .This avoids the CPU intervention and helps maximize system performance by off-loading the CPU. There are 12 DMA channels in the H5 processor. Each DMA channel can generate interrupts. According to different pending status, the referenced DMA channel generates corresponding interrupt. And the configuration information of every DMA channel stores in the DDR or SRAM. When start a DMA transfer, the **DMA Channel Descriptor Address Register** contains the address information in the DDR or SRAM, where has the relevance configuration information of the DMA transfers.

Features:

- DMA transfer supports in either direction between memory and peripheral, between peripheral and memory, or between memory and memory.
- Transfers data width of 8/16/32/64-bit
- 12 DMA channels
- Programs the DMA burst size
- Flexible data source and destination address generation
- Supports linear and IO address modes
- Interrupt generated for each DMA channel

4.11.2. Block Diagram

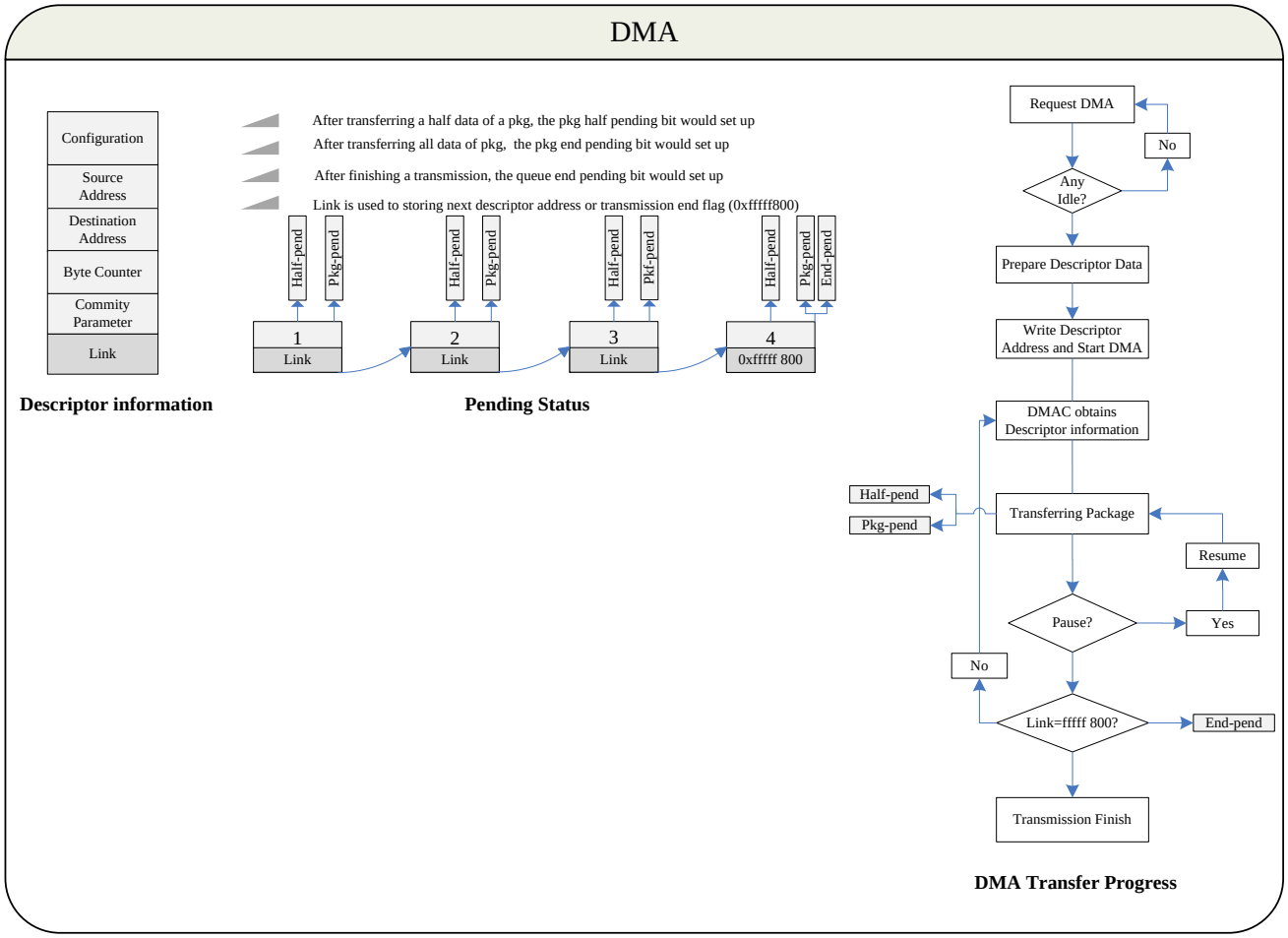


Figure 4-16. DMA Block Diagram

4.11.3. Functionalities Description

4.11.3.1. DRQ Type and Corresponding Relation

Table 4-2. DMA DRQ Table

Source DRQ Type		Destination DRQ Type	
Port NO.	**Module Name**	**Port NO.**	**Module Name**
Port 0	SRAM	Port 0	SRAM
Port 1	SDRAM	Port 1	SDRAM
Port 2	/	Port 2	OWA_TX
Port 3	I2S/PCM 0_RX	Port 3	I2S/PCM 0_TX
Port 4	I2S/PCM 1_RX	Port 4	I2S/PCM 1_TX
Port 5	NAND	Port 5	NAND

Port 6	UART0_RX	Port 6	UART0_TX
Port 7	UART1_RX	Port 7	UART1_TX
Port 8	UART2_RX	Port 8	UART2_TX
Port 9	UART3_RX	Port 9	UART3_TX
Port 10	/	Port 10	/
Port 11	/	Port 11	/
Port 12	/	Port 12	/
Port 13	/	Port 13	/
Port 14	/	Port 14	/
Port 15	Audio Codec_ADC	Port 15	Audio Codec_DAC
Port 16	/	Port 16	/
Port 17	USB OTG_Device_EP1	Port 17	USB OTG_Device_EP1
Port 18	USB OTG_Device_EP2	Port 18	USB OTG_Device_EP2
Port 19	USB OTG_Device_EP3	Port 19	USB OTG_Device_EP3
Port20	USB OTG_Device_EP4	Port 20	USB OTG_Device_EP4
Port 21	/	Port 21	/
Port 22	/	Port 22	/
Port 23	SPI0_RX	Port 23	SPI0_TX
Port 24	SPI1_RX	Port 24	SPI1_TX
Port 25		Port 25	
Port 26		Port 26	
Port 27		Port 27	I2S/PCM 2_TX
Port 28		Port 28	
Port 29		Port 29	
Port 30		Port 30	

4.11.3.2. DMA Descriptor

In this section, the DMA descriptor registers will be introduced in detail.

When started a DMA transmission, the module data are transferred as packages, which has the link data information. And, by reading the **DMA Status Register**, the status of a DMA channel could be known. Reading back the **DMA Channel Descriptor Address Register**, the value is the link data in the transferring package. If only the value is equal to 0xfffff800, then it can be regarded as NULL, which means the package is the last package in this DMA transmission. Otherwise, the value means the start address of the next package. And, the **DMA Channel Descriptor Address Register** can be changed during a package transferring.

When transferring the half of a package, the relevant pending bit will be set up automatically, and if the corresponding interrupt is enabled, DMA generates an interrupt to the system. The similar thing would occur when transferring a package completely. Meanwhile, if DMA has transferred the last package in the data, the relevant pending bit would be set up, and generates an interrupt if the corresponding interrupt is enabled. The flow-process diagram is shown in **DMA Block Diagram**.

During a DMA transmission, the configuration could be obtained by the **DMA Channel Configuration Register**. And

behind the address of the configuration register in DDR or SRAM, there are some registers including other information of a DMA transmission. The structure chart is shown in **DMA Block Diagram**. Also, other information of a transferring data can be obtained by reading the **DMA Channel Current Source Address Register** , **DMA Channel Current Destination Address Register** and **DMA Channel Byte Counter Left Register**. The configuration must be word-aligning.

The transferring data would be paused when setting up the **DMA Channel Pause Register**, if coming up emergency. And the pausing data could be presumable when setting 0 to the same bit in the **DMA Channel Pause Register**.

4.11.4. Register List

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register1
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register0
DMA_IRQ_PEND_REG1	0x0014	DMA IRQ Pending Register1
DMA_SEC_REG	0x0020	DMA Security Register
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x0040	DMA Channel Enable Register (N=0~11)
DMA_PAU_REG	0x0100+0x0004+N*0x0040	DMA Channel Pause Register (N=0~11)
DMA_DESC_ADDR_REG	0x0100+0x0008+N*0x0040	DMA Channel Start Address Register (N=0~11)
DMA_CFG_REG	0x0100+0x000C +N*0x0040	DMA Channel Configuration Register (N=0~11)
DMA_CUR_SRC_REG	0x0100+0x0010+N*0x0040	DMA Channel Current Source Register (N=0~11)
DMA_CUR_DEST_REG	0x0100+0x0014+N*0x0040	DMA Channel Current Destination Register (N=0~11)
DMA_BCNT_LEFT_REG	0x0100+0x0018+N*0x0040	DMA Channel Byte Counter Left Register (N=0~11)
DMA_PARA_REG	0x0100+0x001C+N*0x0040	DMA Channel Parameter Register (N=0~11)
DMA_MODE_REG	0x0100+0x0028+N*0x0040	DMA Mode Register (N=0~11)
DMA_FDESC_ADDR_REG	0x0100+0x002C+N*0x0040	DMA Formar Descriptor Address Register (N=0~11)
DMA_PKG_NUM_REG	0x0100+0x0030+N*0x0040	DMA Package Number Register (N=0~11)

4.11.5. Register Description

4.11.5.1. DMA IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable.

			0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable.
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable.

			0: Disable 1: Enable

4.11.5.2. DMA IRQ Enable Register1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA 10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA 10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA10_HLAF_IRQ_EN DMA 10 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA 9 Queue End Transfer Interrupt Enable. 0: Disable

			1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA 9 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA 9 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA 8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA 8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA 8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

4.11.5.3. DMA IRQ Pending Status Register0 (Default Value: 0x0000_0000)

Offset:0x0010			**Register Name: DMA_IRQ_PEND_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
29	R/W1C	0x0	DMA7_PKG_IRQ_ PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect

			1: Pending.
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
19	/	/	/

18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_ PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
9	R/W1C	0x0	DMA2_PKG_IRQ_ PEND

			DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
5	R/W1C	0x0	DMA1_PKG_IRQ_ PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending.

			Setting 1 to the bit will clear it. 0: No effect 1: Pending.

4.11.5.4. DMA IRQ Pending Status Register1 (Default Value: 0x0000_0000)

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_ PEND DMA 10 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it.

			0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_ PEND DMA 9 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA 8 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_ PEND DMA 8 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA 8 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

4.11.5.5. DMA Security Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: DMA_SECURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DMA11_SECURE DMA Channel 11 Security. 0: Secure 1: Non-secure
10	R/W	0x0	DMA10_SECURE DMA Channel 10 Security. 0: Secure 1: Non-secure
9	R/W	0x0	DMA9_SECURE DMA Channel 9 Security. 0: Secure 1: Non-secure
8	R/W	0x0	DMA8_SECURE DMA Channel 8 Security. 0: Secure 1: Non-secure
7	R/W	0x0	DMA7_SECURE DMA Channel 7 Security. 0: Secure 1: Non-secure
6	R/W	0x0	DMA6_SECURE DMA Channel 6 Security. 0: Secure 1: Non-secure
5	R/W	0x0	DMA5_SECURE DMA Channel 5 Security. 0: Secure 1: Non-secure
4	R/W	0x0	DMA4_SECURE. DMA Channel 4 Security. 0: Secure 1: Non-secure

3	R/W	0x0	DMA3_SECURE. DMA Channel 3 Security. 0: Secure 1: Non-secure
2	R/W	0x0	DMA2_SECURE. DMA Channel 2 Security. 0: Secure 1: Non-secure
1	R/W	0x0	DMA1_SECURE. DMA Channel 1 Security. 0: Secure 1: Non-secure
0	R/W	0x0	DMA0_SECURE. DMA Channel 0 Security. 0: Secure 1: Non-secure

4.11.5.6. DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

4.11.5.7. DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	MBUS FIFO Status 0:Empty 1:Not Empty
29:12	/	/	/
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy

4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy.
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy.
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle, 1: Busy.
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle, 1: Busy.
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle, 1: Busy.

4.11.5.8. DMA Channel Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0040 (N=0~11)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable.

4.11.5.9. DMA Channel Pause Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0004+N*0x0040 (N=0~11)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE.

			Pausing DMA Channel Transfer Data. 0: Resume Transferring, 1: Pause Transferring.

4.11.5.10. DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0008+N*0x0040 (N=0~11)			Register Name: DMA_DESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMA_DESC_ADDR DMA Channel Descriptor Address. The Descriptor Address must be word-aligned.

4.11.5.11. DMA Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x000C+N*0x0040 (N=0~11)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	/	/	/
23:22	R	0x0	DMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1 01: 4 10: 8 11: 16
21	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode
20:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details is in **DMA DRQ Table**.

15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	/	/	/
7:6	R	0x0	DMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: 4 10: 8 11: 16
5	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
4:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details is in **DMA DRQ Table**.

4.11.5.12. DMA Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0010+N*0x0040 (N=0~11)			**Register Name: DMA_CUR_SRC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

4.11.5.13. DMA Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0014+N*0x0040 (N=0~11)			**Register Name: DMA_CUR_DEST_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

4.11.5.14. DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0018+N*0x0040 (N=0~11)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

4.11.5.15. DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x001C+N*0x0040 (N=0~11)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles n.

4.11.5.16. DMA Mode Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0028+N*0x0040 (N=0~11)			Register Name: DMA_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE. 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

4.11.5.17. DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x002C+N*0x0040 (N=0~11)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to store the former value of **DMA Channel Descriptor Address Register**.

4.11.5.18. DMA Package Number Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0030+N*0x0040 (N=0~11)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

4.12. GIC

4.12.1. Interrupt Source

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	UART 0	0x0080	UART 0 interrupt
33	UART 1	0x0084	UART 1 interrupt
34	UART 2	0x0088	UART 2 interrupt
35	UART 3	0x008C	UART 3 interrupt

36	/	0x0090	/
37	/	0x0094	/
38	TWI 0	0x0098	TWI 0 interrupt
39	TWI 1	0x009C	TWI 1 interrupt
40	TWI 2	0x00A0	TWI 2 interrupt
41	/	0x00A4	/
42	/	0x00A8	/
43	PA_EINT	0x00AC	PA interrupt
44	OWA	0x00B0	OWA interrupt
45	I2S/PCM-0	0x00B4	I2S/PCM-0 interrupt
46	I2S/PCM-1	0x00B8	I2S/PCM-1 interrupt
47	I2S/PCM-2	0x00BC	I2S/PCM-2 interrupt
48	/	0x00C0	/
49	PF_EINT	0x00C4	PF_EINT interrupt
50	Timer 0	0x00C8	Timer 0 interrupt
51	Timer 1	0x00CC	Timer 1 interrupt
52	/	0x00D0	/
53	/	0x00D4	/
54	/	0x00D8	/
55	PG_EINT	0x00DC	PG_EINT interrupt
56	/	0x00E0	/
57	Watchdog	0x00E4	Watchdog interrupt
58	/	0x00E8	/
59	/	0x00EC	/
60	/	0x00F0	/
61	Audio Codec	0x00F4	Audio Codec interrupt
62	KEYADC	0x00F8	KEYADC interrupt
63	THS	0x00FC	Thermal Sensor interrupt
64	External NMI	0x0100	External Non-Mask Interrupt
65	R_timer 0	0x0104	R_timer 0 interrupt
66	R_timer 1	0x0108	R_timer 1 interrupt
67	/	0x010C	/
68	R_watchdog	0x0110	R_watchdog interrupt
69	R_CIR-RX	0x0114	R_CIR-RX interrupt
70	R_UART	0x0118	R_UART interrupt
71	/	0x011C	/
72	R_Alarm 0	0x0120	R_Alarm 0 interrupt
73	R_Alarm 1	0x0124	R_Alarm 1 interrupt
74	R_Timer 2	0x0128	R_timer 2 interrupt
75	R_Timer 3	0x012C	R_timer 3 interrupt
76	R_TWI	0x0130	R_TWI interrupt
77	R_PL_EINT	0x0134	R_PL_EINT interrupt
78	R_TWD	0x0138	R_TWD interrupt
79	/	0x013C	/

80	/	0x0140	/
81	M-box	0x0144	Message-box interrupt
82	DMA	0x0148	DMA channel interrupt
83	HS Timer	0x014C	HS Timer interrupt
84	/	0x0150	/
85	/	0x0154	/
86	/	0x0158	/
87	/	0x015C	/
88	SMC	0x0160	SMC interrupt
89	/	0x0164	/
90	VE	0x0168	VE interrupt
91	/	0x016C	/
92	SMHC 0	0x0170	SD/MMC Host Controller 0 interrupt
93	SMHC 1	0x0174	SD/MMC Host Controller 1 interrupt
94	SMHC 2	0x0178	SD/MMC Host Controller 2 interrupt
95	/	0x017C	/
96	/	0x0180	/
97	SPI 0	0x0184	SPI 0 interrupt
98	SPI 1	0x0188	SPI 1 interrupt
99	/	0x018C	/
100	/	0x0190	/
101	DRAM_MDFS	0x0194	DRAM_MDFS interrupt
102	NDFC	0x0198	NAND Flash Controller interrupt
103	USB-OTG_Device	0x019C	USB-OTG_Device interrupt
104	USB-OTG_EHCI0	0x01A0	USB-OTG_EHCI0 interrupt
105	USB-OTG_OHCI0	0x01A4	USB-OTG_OHCI0 interrupt
106	USB-EHCI1	0x01A8	USB-EHCI1 interrupt
107	USB-OHCI1	0x01AC	USB-OHCI1 interrupt
108	USB-EHCI2	0x01B0	USB-EHCI2 interrupt
109	USB-OHCI2	0x01B4	USB-OHCI2 interrupt
110	USB-EHCI3	0x01B8	USB-EHCI3 interrupt
111	USB-OHCI3	0x01BC	USB-OHCI3 interrupt
112	CE_S	0x01C0	CE_S interrupt
113	TSC	0x01C4	TSC interrupt
114	EMAC	0x01C8	EMAC interrupt
115	SCR0	0x01CC	SCR0 interrupt
116	CSI	0x01D0	CSI interrupt
117	CSI_CCI	0x01D4	CSI_CCI interrupt
118	TCON0	0x01D8	TCON0 Controller interrupt
119	TCON1	0x01DC	TCON1 Controller interrupt
120	HDMI	0x01E0	HDMI interrupt
121	SCR1	0x01E4	SCR1 interrupt
122	/	0x01E8	/
123	/	0x01EC	/

124	TVE	0x01F0	TVE interrupt
125	DIT	0x01F4	DIT interrupt
126	CE_NS	0x01F8	CE_NS interrupt
127	DE	0x01FC	DE interrupt
128	GPU_GP	0x0200	GPU_GP interrupt
129	GPU_GPMMU	0x0204	GPU_GPMMU interrupt
130	GPU_PMU	0x0208	GPU_PMU interrupt
131	GPU_PP	0x020C	GPU_PP interrupt
132	GPU_PP0	0x0210	GPU_PP0 interrupt
133	GPU_PPMMU0	0x0214	GPU_PPMMU0 interrupt
134	GPU_PP1	0x0218	GPU_PP1 interrupt
135	GPU_PPMMU1	0x021C	GPU_PPMMU1 interrupt
136	GPU_PP2	0x0220	GPU_PP2 interrupt
137	GPU_PPMMU2	0x0224	GPU_PPMMU2 interrupt
138	GPU_PP3	0x0228	GPU_PP3 interrupt
139	GPU_PPMMU3	0x022C	GPU_PPMMU3 interrupt
140	CTI0	0x0230	CTI0 interrupt
141	CTI1	0x0234	CTI1 interrupt
142	CTI2	0x0238	CTI2 interrupt
143	CTI3	0x023C	CTI3 interrupt
144	COMMTX0	0x0240	COMMTX0 interrupt
145	COMMTX1	0x0244	COMMTX1 interrupt
146	COMMTX2	0x0248	COMMTX2 interrupt
147	COMMTX3	0x024C	COMMTX3 interrupt
148	COMMRX0	0x0250	COMMRX0 interrupt
159	COMMRX1	0x0254	COMMRX1 interrupt
150	COMMRX2	0x0258	COMMRX2 interrupt
151	COMMRX3	0x025C	COMMRX3 interrupt
152	PMU0	0x0260	PMU0 interrupt
153	PMU1	0x0264	PMU1 interrupt
154	PMU2	0x0268	PMU2 interrupt
155	PMU3	0x026C	PMU3 interrupt
156	AXI_ERROR	0x0270	AXI_ERROR interrupt

Note: For details about GIC, please refer to the ***GIC PL400 technical reference manual*** and ***ARM GIC Architecture Specification V2.0***.

4.13. Message Box

4.13.1. Overview

Message Box provides a MSGBox-interrupt mechanism for on-chip processors intercommunication.

The MSGBox-interrupt mechanism allows the software to establish a communication channel between the two users through a set of registers and associated interrupt signals by sending or receiving messages.

Features:

- Two users for Message Box instance(User0 for CPUS and User1 for CPU0/CPU1)
- Eight Message Queues for the MSGBox instance
- Each of Queues could be configured as transmitter or receiver for user
- Two interrupts (one per user) for the MSGBox instance
- Register polling for the MSGBox instance
- 32-bit message width
- Four-message FIFO depth for each message queue

4.13.2. Block Diagram

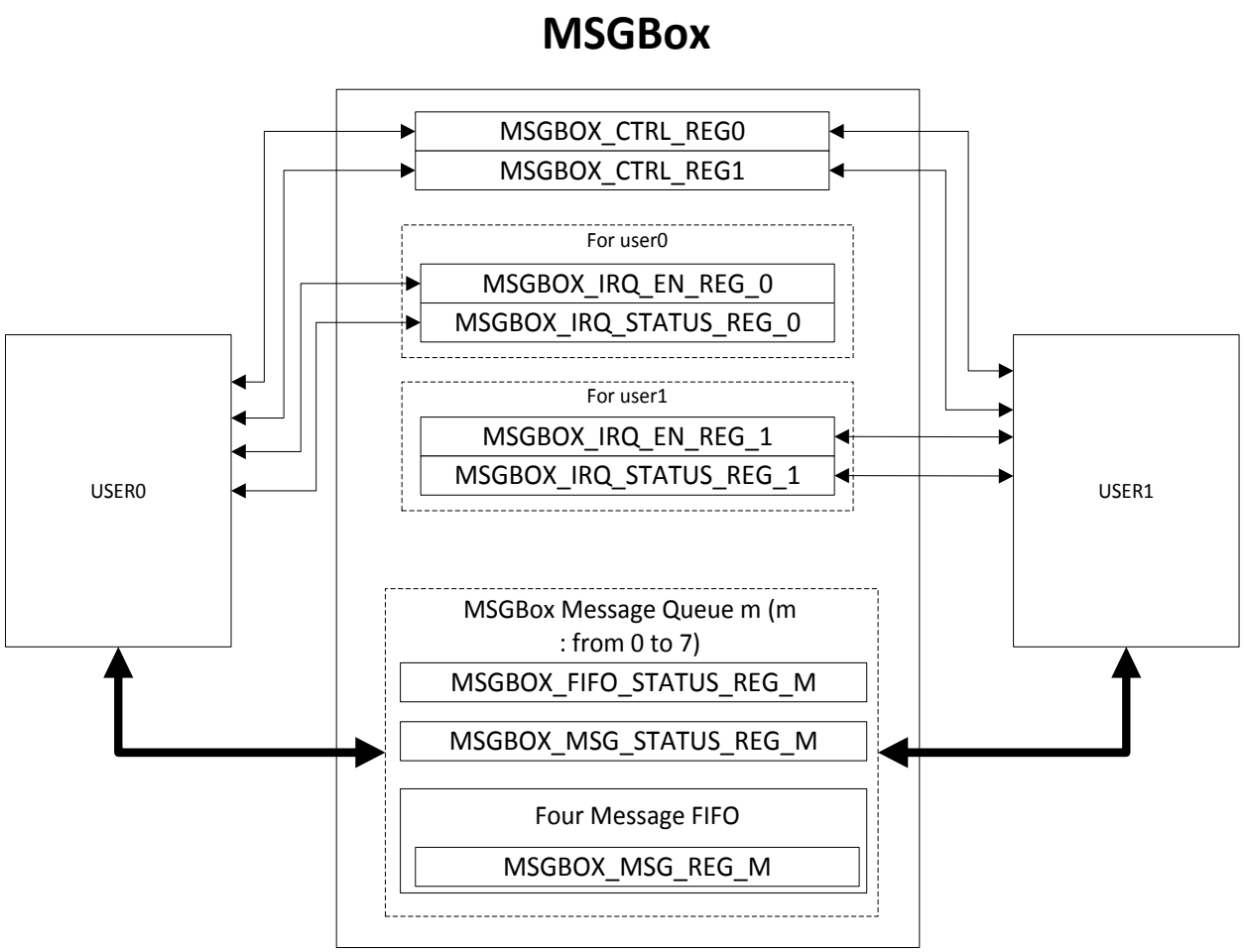


Figure 4-17. Message Box Block Diagram

4.13.3. Operations and Functional Descriptions

4.13.3.1. Typical Applications

Figure 4-18. Message Box Typical Application Chart

4.13.3.2. Message Queue Assignment

To transmit messages from a user to the other user through any Message Queue, set the corresponding bit in the **MSGBOX_CTRL_REG0**/**MSGBOX_CTRL_REG1** register.

When a 32-bit message is written to the **MSGBOXN_MSG_REG** register (N is the message queue number, N=0~7), the message is appended into the FIFO queue. This queue holds 4 messages. If the queue is full, the message is discarded. The receiver user could read the **MSGBOXN_MSG_REG** register to retrieve a message from the corresponding Message Queue FIFO.

It is recommended that register polling be used for a user to send a message:

- Set a Message Queue as a transmitter (in the **MSGBOX_CTRL_REG0**/**MSGBOX_CTRL_REG1** register).
- Check the FIFO status or the message status (in the **MSGBOXN_FIFO_STATUS_REG** or **MSGBOXN_MSG_STATUS_REG**).
- Write the message to the corresponding **MSGBOXN_MSG_REG** register, if space is available.

The transmit interrupt might be used when the initial MSGBox status indicates that the Message Queue is full. In this case, the sender can enable the corresponding **MSGBOXU_IRQ_EN_REG** interrupt for the user. This allows the user to be notified by interrupt when the message queue is not full.

4.13.3.3. Interrupt Request

An interrupt request allows the user of the MSGBox to be notified when a new message is received or when the message queue is not full.

An event can generate an interrupt request when enable the corresponding bit in the **MSGBOXU_IRQ_EN_REG** (U is the user number, U=0~1) register. Events are reported in the appropriate **MSGBOXU_IRQ_STATUS_REG** register.

An event stops generating interrupt requests when disable the corresponding bit in the **MSGBOXU_IRQ_EN_REG** register.

In case of the **MSGBOXU_IRQ_STATUS_REG** register, the event is reported in the corresponding bit even if the interrupt request generation is disabled for this event.

4.13.4. Register List

Module Name	Base Address
MSGBOX	0x01C17000

Register Name	Offset	Description
MSGBOX_CTRL_REG0	0x0000	Message Queue Attribute Control Register 0
MSGBOX_CTRL_REG1	0x0004	Message Queue Attribute Control Register 1

MSGBOXU_IRQ_EN_REG	0x0040+N*0x0020 (N=0,1)	IRQ Enable for User U
MSGBOXU_IRQ_STATUS_REG	0x0050+N*0x0020 (N=0,1)	IRQ Status for User U
MSGBOXN_FIFO_STATUS_REG	0x0100+N*0x0004 (N = 0~7)	FIFO Status for Message Queue N
MSGBOXN_MSG_STATUS_REG	0x0140+N*0x0004 (N = 0~7)	Message Status for Message Queue N
MSGBOXN_MSG_REG	0x0180+N*0x0004 (N = 0~7)	Message Register for Message Queue N

4.13.5. Register Description

4.13.5.1. MSGBox Control Register 0(Default Value: 0x1010_1010)

Offset: 0x0000			Register Name: MSGBOX_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ3. Message Queue 3 is a transmitter of user u. 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ3. Message Queue 3 is a receiver of user u. 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ2. Message Queue 2 is a transmitter of user u. 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ2. Message Queue 2 is a receiver of user u. 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ1

			Message Queue 1 is a transmitter of user u. 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ1. Message Queue 1 is a receiver of user u. 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ0. Message Queue 0 is a transmitter of user u. 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ0. Message Queue 0 is a receiver of user u. 0: user0 1: user1

4.13.5.2. MSGBox Control Register 1(Default Value: 0x1010_1010)

Offset: 0x0004			Register Name: MSGBOX_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ7. Message Queue 7 is a transmitter of user u. 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ7. Message Queue 7 is a receiver of user u. 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ6. Message Queue 6 is a transmitter of user u. 0: user0

			1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ6. Message Queue 6 is a receiver of user u. 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ5 Message Queue 5 is a transmitter of user u. 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ5. Message Queue 5 is a receiver of user u. 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ4. Message Queue 4 is a transmitter of user u. 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ4. Message Queue 4 is a receiver of user u. 0: user0 1: user1

4.13.5.3. MSGBox IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0040+N*0x0020 (N=0,1)			Register Name: MSGBOXU_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	TRANSMIT_MQ7_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 is not full.)
14	R/W	0x0	RECEPTION_MQ7_IRQ_EN. 0: Disable

			1: Enable (It will notify user u by interrupt when Message Queue 7 has received a new message.)
13	R/W	0x0	TRANSMIT_MQ6_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 is not full.)
12	R/W	0x0	RECEPTION_MQ6_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 has received a new message.)
11	R/W	0x0	TRANSMIT_MQ5_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 is not full.)
10	R/W	0x0	RECEPTION_MQ5_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 has received a new message.)
9	R/W	0x0	TRANSMIT_MQ4_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 is not full.)
8	R/W	0x0	RECEPTION_MQ4_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 has received a new message.)
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 is not full.)
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 has received a new message.)
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 is not full.)
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN. 0: Disable

			1: Enable (It will notify user u by interrupt when Message Queue 2 has received a new message.)
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 is not full.)
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 has received a new message.)
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 is not full.)
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN. 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 has received a new message.)

4.13.5.4. MSGBox IRQ Status Register u(Default Value: 0x0000_AAAA)

Offset:0x0050+N*0x0020 (N=0,1)			Register Name: MSGBOXU_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W1C	0x1	TRANSMIT_MQ7_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 is not full. Setting 1 to this bit will clear it.
14	R/W1C	0x0	RECEPTION_MQ7_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 has received a new message. Setting 1 to this bit will clear it.
13	R/W1C	0x1	TRANSMIT_MQ6_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 is not full. Setting 1 to this bit will clear it.
12	R/W1C	0x0	RECEPTION_MQ6_IRQ_PEND. 0: No effect

			1: Pending. This bit will be pending for user u when Message Queue 6 has received a new message. Setting 1 to this bit will clear it.
11	R/W1C	0x1	TRANSMIT_MQ5_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 is not full. Setting 1 to this bit will clear it.
10	R/W1C	0x0	RECEPTION_MQ5_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 has received a new message. Setting 1 to this bit will clear it.
9	R/W1C	0x1	TRANSMIT_MQ4_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 is not full. Setting 1 to this bit will clear it.
8	R/W1C	0x0	RECEPTION_MQ4_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 has received a new message. Setting 1 to this bit will clear it.
7	R/W1C	0x1	TRANSMIT_MQ3_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 is not full. Setting 1 to this bit will clear it.
6	R/W1C	0x0	RECEPTION_MQ3_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 has received a new message. Setting 1 to this bit will clear it.
5	R/W1C	0x1	TRANSMIT_MQ2_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 is not full. Setting 1 to this bit will clear it.
4	R/W1C	0x0	RECEPTION_MQ2_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 has received a new message. Setting 1 to this bit will clear it.
3	R/W1C	0x1	TRANSMIT_MQ1_IRQ_PEND. 0: No effect

			1: Pending. This bit will be pending for user u when Message Queue 1 is not full. Setting 1 to this bit will clear it.
2	R/W1C	0x0	RECEPTION_MQ1_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 has received a new message. Setting 1 to this bit will clear it.
1	R/W1C	0x1	TRANSMIT_MQ0_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 is not full. Setting 1 to this bit will clear it.
0	R/W1C	0x0	RECEPTION_MQ0_IRQ_PEND. 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 has received a new message. Setting 1 to this bit will clear it.

4.13.5.5. MSGBox FIFO Status Register m(Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~7)			Register Name: MSGBOXN_FIFO_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 1	/	/	/
0	R	0x0	FIFO_FULL_FLAG. 0: The Message FIFO queue is not full (space is available). 1: The Message FIFO queue is full. This FIFO status register has the status related to the message queue.

4.13.5.6. MSGBox Message Status Register m(Default Value: 0x0000_0000)

Offset:0x0140+N*0x0004 (N=0~7)			Register Name: MSGBOXN_MSG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	MSG_NUM. Number of unread messages in the message queue. Here, limit to four messages per message queue. 000: There is no message in the message FIFO queue. 001: There is 1 message in the message FIFO queue. 010: There are 2 messages in the message FIFO queue. 011: There are 3 messages in the message FIFO queue.

			100: There are 4 messages in the message FIFO queue. 101~111:/

4.13.5.7. MSGBox Message Queue Register (Default Value: 0x0000_0000)

Offset:0x0180+N*0x0004 (N=0~7)			Register Name: MSGBOXN_MSG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

4.14. Spinlock

4.14.1. Overview

Spinlock provides hardware assistance for synchronizing the processes running on multiple processors in the device. The SpinLock implements thirty-two 32-bit spinlocks (or hardware semaphores), which provides an efficient way to perform a lock operation of a device resource using a single read access, and avoid the need for a 'read-modify-write' bus transfer that not all the programmable cores are capable of.

Spinlocks are present to solve the need for synchronization and mutual exclusion between heterogeneous processors and those not operating under a single, shared operating system. There is no alternative mechanism to accomplish these operations between processors in separate subsystems. However, Spinlocks do not solve all system synchronization issues. They have limited applicability and should be used with care to implement higher level synchronization protocols.

A spinlock is appropriate for mutual exclusion for access to a shared data structure. It should be used only when:

1) The time to hold the lock is predictable and small (for example, a maximum hold time of less than 200 CPU cycles may be acceptable).
2) The locking task can not be preempted, suspended, or interrupted while holding the lock (this would make the hold time large and unpredictable).
3) The lock is lightly contended, that is the chance of any other process (or processor) trying to acquire the lock while it is held is small.

If the conditions are not met, then a spinlock is not a good candidate. One alternative is to use a spinlock for critical section control (engineered to meet the conditions) to implement a higher level semaphore that can support preemption, notification, timeout or other higher level properties.

Features:

- Spinlock module includes 32 spinlocks
- Two kinds of status of lock register: TAKEN and NOT TAKEN

4.14.2. Operations and Functional Descriptions

4.14.2.1. Typical Applications

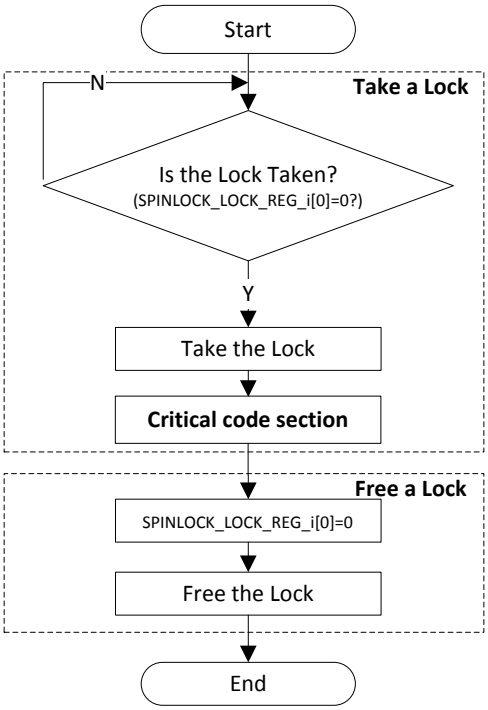


Figure 4-19. Spinlock Typical Application Flow Chart

4.14.2.2. Lock Register State Diagram

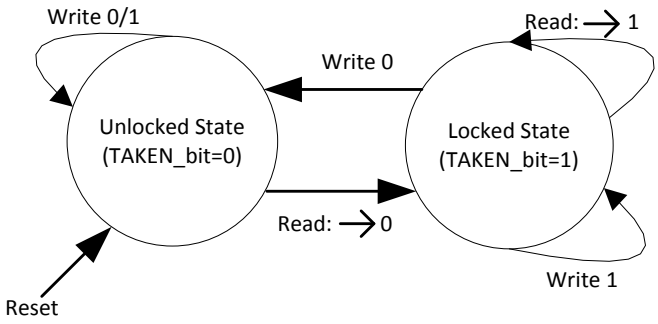


Figure 4-20. Spinlock Lock Register State Diagram

Every lock register has two kinds of states: TAKEN(locked) or NOT TAKEN(Unlocked). Only read-0-access and write-0-access could change the state of lock register and the other accesses have no effect. Just 32-bit read and write are supported to access all lock registers.

4.14.2.3. Spinlock Clock Gating and Software Reset

Spinlock clock gating should be open before using it. Setting the bit[22] of **Bus Clock Gating Register1** to 1 could activate Spinlock and then de-asserting its software reset. Setting the bit[22] of **Bus Software Reset Register 1** to 1 could de-assert the software reset of Spinlock. If it is no need to use spinlock, both the gating bit and software reset bit should be set 0.

4.14.2.4. Take and Free a Spinlock

Checking out **Spinlock Register Status** is necessary when a processor would like to take a spinlock. This register stores the status of all 32 lock registers: TAKEN or NOT TAKEN(free).

In order to request to take a spinlock, a processor has to do a read-access to the corresponding lock register. If lock register returns 0, the processor takes this spinlock. And if lock register returns 1, the processor must retry.

Writing 0 to a lock register frees the corresponding spinlock. If the lock register is not taken, write-access has no effect. For a taken spinlock, every processor has the privilege to free this spinlock. But it is suggested that the processor which has taken the spinlock free it for strictness.

4.14.3. Programming Guidelines

Take CPU0's synchronization with CPUS with Spinlock0 for an example, CPU0 takes the spinlock0 firstly in the instance：

CPU0

Step 1: CPU0 initializes Spinlock

```
writel(readl(Bus Clock Gating Register1)|(1<<22) , Bus Clock Gating Register1);    //open Spinlock clock gating
writel (readl(Bus Software Reset Register 1)|(1<<22) , Bus Software Reset Register 1);    //software reset Spinlock
```

Step 2: CPU0 requests to take spinlock0

```
rdata=readl(SPINLOCK_SYSTATUS_REG);                          //check lock register0 status, if it is taken, check till
if(rdata != 0)    rdata=readl(SPINLOCK_SYSTATUS_REG);        // lock register0 is free
                  ⋮
rdata=readl(SPINLOCKN_LOCK_REG);                             //request to take spinlock0, if fail, retry till
if(rdata != 0)    rdata=readl(SPINLOCKN_LOCK_REG);           // lock register0 is taken
                  ⋮
 ---------- CPU0 critical code section ----------
```

Step 3: CPU0 free spinlock0

```
writel (0, SPINLOCKN_LOCK_REG);                              //CPU0 frees spinlock0
```

Step 4: CPU0 waits for CPUS' freeing spinlock0

```
writel (readl(SPINLOCK_STATUS_REG) == 1);                    // CPU0 waits for CPUS'  freeing spinlock0
```


CPUS

Step 1: CPU0 has taken spinlock0, CPUS waits for CPU0' freeing spinlock0
while(readl(**SPINLOCK_STATUS_REG**) == 1); // CPUS waits for CPU0' freeing spinlock0

Step 2: CPUS takes spinlock0 and go on
---------- CPUS critical code section ----------

Step 3: CPUS frees spinlock0
writel (0, **SPINLOCKN_LOCK_REG**); //CPUS frees spinlock0

4.14.4. Register List

Module Name	Base Address
SPINLOCK	0x01C18000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_LOCK_REGN	0x0100+N*0x0004	Spinlock Register N (N=0~31)

4.14.5. Register Description

4.14.5.1. Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM. Number of lock registers implemented. 00: This instance has 32 lock registers. 01: This instance has 64 lock registers. 10: This instance has 128 lock registers. 11: This instance has 256 lock registers.
27:16	/	/	/
15:9	/	/	/
8	R	0x0	IU0. In-Use flag0, covering lock register0-31.

			0: All lock register 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

4.14.5.2. Spinlock Register Status (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS. SpinLock[i] status (i=0~31) 0: The Spinlock is free 1: The Spinlock is taken.

4.14.5.3. Spinlock Register N (N=0 to 31)(Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TAKEN. Lock State. Read 0x0: The lock was previously Not Taken (free).The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

4.15. Crypto Engine

4.15.1. Overview

The Crypto Engine(CE) is one encrypt/decrypt function accelerator. It is suitable for a variety of applications. It can support encryption ,decryption and calculate the hash value. Several algorithm modes are supported by the Crypto Engine. The Crypto Engine has a special internal DMA(IDMA) controller to transfer data .

The Crypto Engine can encrypt or decrypt a large amount of data. And it can encrypt and decrypt one or more blocks at one time.

Features:

- Supports symmetrical algorithm :AES, DES, TDES
- Supports asymmetrical algorithm :RSA512/1024/2048-bit
- Supports secure Hash algorithm: MD5, SHA-1,SHA-224,SHA-256, HMAC
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Supports ECB, CBC, CTR modes for DES/TDES
- Supports ECB, CBC, CTR, CTS modes for AES
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports multi-package mode for MD5/SHA-1/SHA-224/SHA-256
- Supports internal DMA controller for data transfer with memory
- Supports secure and non-secure interface respectively

4.15.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

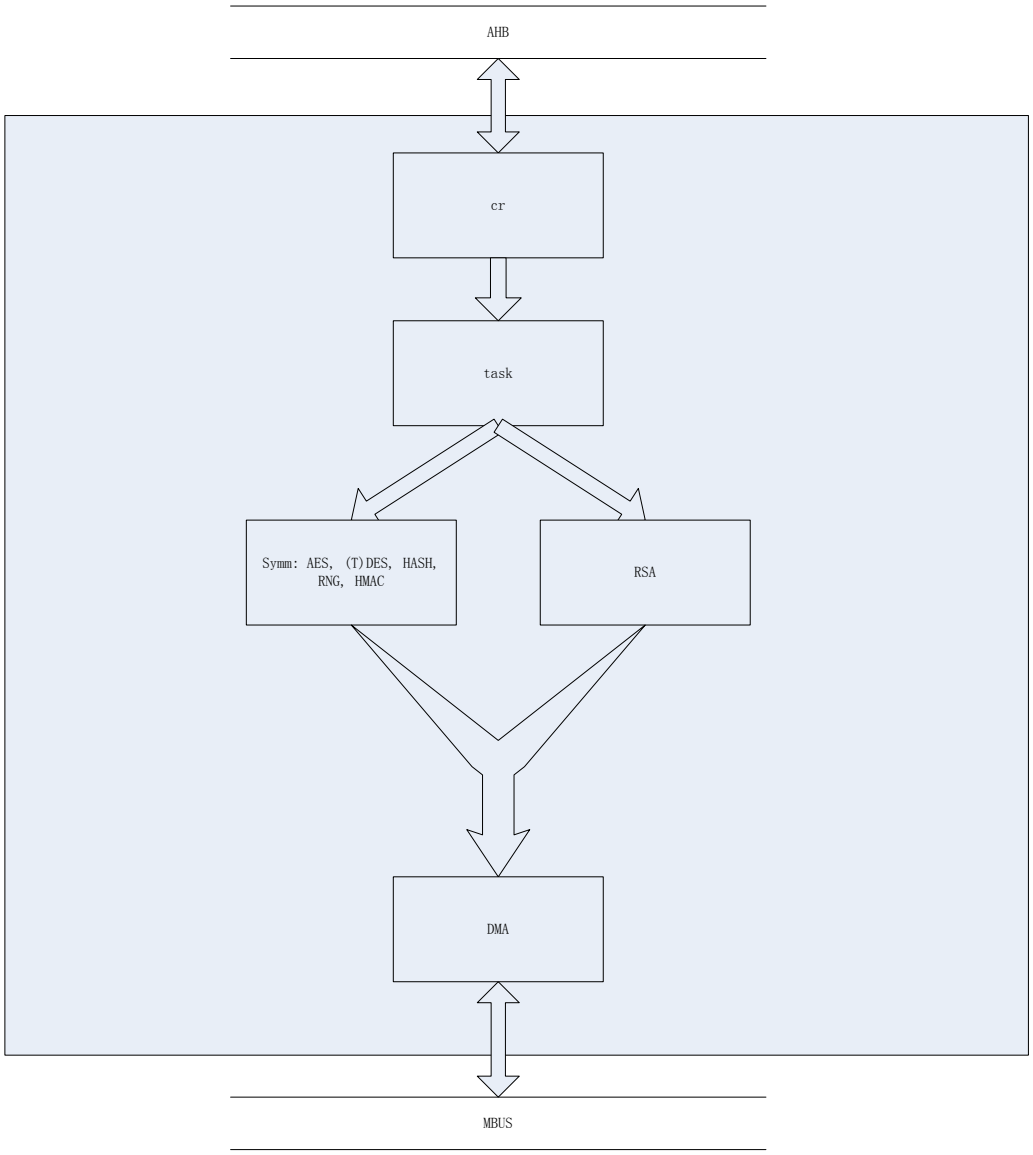


Figure 4-21. CE Block Diagram

4.15.3. Operations and Functional Descriptions

4.15.3.1. Crypto Engine Task Descriptor

Crypto Engine task deccriptor is 44*4 Byte memory. Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

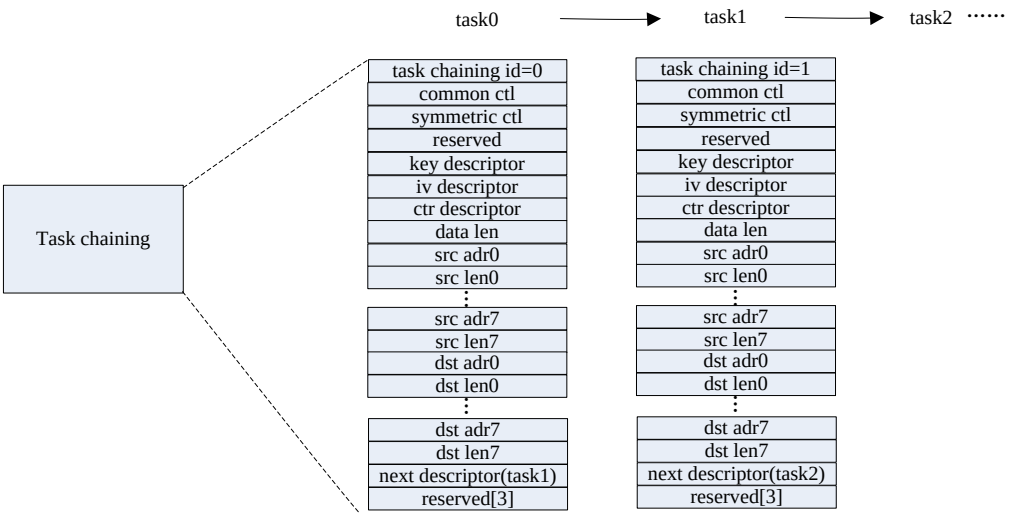


Figure 4-22. Crypto Engine Task Chaining

Task chaining id supports 0~3.

4.15.3.2. Task_descriptor_queue Common Control

Bit	Description
31	INTERRUPT_ENABLE Interrupt enable for current task 0: Disable interrupt 1: Enable interrupt
30:17	/
16	IV_MODE IV mode for SHA-1/SHA-224/SHA-256 /MD5 or constants 0: Use initial constants defined in FIPS-180 1: Use input iv
15	HMAC_PLAINTEXT_LAST_FLAG 0: Not the last HMAC plaintext package 1: The last HMAC plaintext package
14:9	/
8	OP_DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/
6:0	ALGORITHM_TYPE

	0: AES 1: DES 2: Triple DES (3DES) 3~15: Reserved 16: MD5 17: SHA-1 18: SHA-224 19: SHA-256 20: Reserved 21: Reserved 22: HMAC-SHA1 23: HMAC-SHA256 24~31: Reserved 32: RSA 33~47: Reserved 48: TRNG 49: PRNG 50~62: Reserved

4.15.3.3. Task_descriptor_queue Symmetric Control

Bit	Description
31:24	/
23:20	KEY_SELECT key select for AES 0000: Select input CE_KEYx (Normal Mode) 0001: Select {SSK} 0010: Select {HUK} 0011: Select {RSSK} 0100-0111: Reserved 1000-1111: Select internal Key n (n from 0 to 7)
19:18	/
17	PRNG_LD Load new 15bits key into lfsr for PRNG
16	AES_CTS_LAST_PACKAGE_FLAG When set to '1', it means this is the last package for AES-CTS mode. (the size of the last package >128bit)
15:12	/
11:8	ALGORITHM_MODE CE Operation Mode

	0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: Ciphertext Stealing (CTS) mode Other: Reserved
7:4	/
3:2	CTR_WIDTH Counter Width for CTR Mode 00: 16-bit Counter 01: 32-bit Counter 10: 64-bit Counter 11: 128-bit Counter
1:0	AES_KEY_SIZE 00: 128-bit 01: 192-bit 10: 256-bit 11: Reserved

4.15.3.4. Task_descriptor_queue Asymmetric Control

Bit	Description
31	/
30:28	RSA_WIDTH RSA Pubic Modulus Width 000: 512 bit 001: 1024 bit 010: 2048 bit Other: Reserved
27:0	/

4.15.3.5. Task Request

Basically, there are 4 steps for one task handling from software. Firstly, software should configure task descriptor in memory, including all fields in descriptor. Channel id corresponds to one channel in CE, from 0 to 3 for secure and non secure world respectively. According to algorithm type, software should set the fields in common control, symmetric control, asymmetric control, then provide key/iv/ctr address and the data length of this task. Source and destination sg address and size are set based on upper application. If there is another task concatenating after this task, then set its descriptor address at next descriptor field. Secondly, software should set registers, including task descriptor address, interrupt control. Thirdly, software read load register to ensure that the bit0 is zero, then starts request by pulled up the bit0 of the load register. Lastly, wait interrupt status.

4.15.3.6. Data Length Setting

Data length field in task descriptor has different meaning for different algorithms. For AES-CTS algorithms mode data length field indicates valid source data byte number, for others indicate source data words number. For PRNG, data length should be 5 words aligned, For TRNG should be 8 words aligned. Data size in source and destination sg is as words, whose value should corresponds with data length field, or else CE will report error and stop execution.

4.15.3.7. Security Operation

When CPU issues request to CE module, CE module will register CPU's secure mode state. When executing this request, this state bit works as access flag for inner and system resource. For HUK/RSSK/SSK from SID, only secure mode can access, or else these keys will be used as 0. For access to SID and keysram module through AHB bus, only secure mode can success, or else will read 0 or can not write. When issuing MBUS read and write requests, CE will use this secure state bit as mprot signal, so certain secure state accesses corresponding memory space, namely secure request can access secure and non secure space, but non secure request only can access non secure space.

4.15.3.8. Error Check

CE module includes error detection for task configuration, data computing error, and authentication invalid. When algorithm type in task description is read into module, CE will check if this type is supported through checking algorithm type field in common ctrl. If type value is out of support scope, CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting task descriptor, input size and output size configuration will be checked to avoid size error. If size configuration is wrong, CE will issue interrupt signal and set error state. To protect keys would be put into keysram from disclose, if request using RSSK is for AES decryption and destination address is not in keysram space, CE would not execute this task. It will issue interrupt signal and set error state.

4.15.3.9. Clock Requirement

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	24MHz ~ 200MHz
m_clk	MBUS clk	24MHz ~ 400MHz
ce_clk	CE work clock	24MHz ~ 300MHz

4.15.4. Register List

Module Name	Base Address

CE_NS	0x01C15000
CE_S	0x01C15800

Register Name	Offset	Description
CE_TDQ	0x0000	Task Descriptor Address
CE_CTR	0x0004	Gating Control Register
CE_ICR	0x0008	Interrupt Control Register
CE_ISR	0x000C	Interrupt Status Register
CE_TLR	0x0010	Task Load Register
CE_ESR	0x0018	Task Error type Register
CE_CSSGR	0x001C	Current Source Scatter Group Register
CE_CDSGR	0x0020	Current Destination Scatter Group Register
CE_CSAR	0x0024	Current Source Address Register
CE_CDAR	0x0028	Current Destination Address Register
CE_TPR	0x002C	Throughput Register

4.15.5. Register Description

4.15.5.1. Crypto Engine Task Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CE_TDA Task Descriptor Address

4.15.5.2. Crypto Engine Control Register (Default Value: UDF)

Offset: 0x0004			Register Name:CE_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	RSA_CLK_GATING RSA CLK Gating Enable(only for S world) 0: RSA clk gating enable 1: RSA clk gating disable
2:0	R	UDF	DIE_ID Die Bonding ID

4.15.5.3. Crypto Engine Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008	Register Name: CE_ICR

Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	TASK_INT_EN Task chaining0~3 interrupt enable 0: Interrupt disable 1: Interrupt enable

4.15.5.4. Crypto Engine Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W1C	0x0	TASK_END_PENDING Task channel0-3 end pending 0: Not finished 1: Finished It indicates whether task has been completed . **Note:** Write '1' to clear it.

4.15.5.5. Crypto Engine Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Task_Load When set , CE starts to load the configure of task from task descriptor queue and start to perform the task if task FIFO is not full.

4.15.5.6. Crypto Engine Task Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R	0x0	TASK_CHANNEL Indicate which channel is running 00: Task channel0 01: Task channel1 10: Task channel2

			11: Task channel3

4.15.5.7. Crypto Engine Error Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W1C	0x0	CH3_ERROR Task channel3 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES 1xxx: Reserved Write '1' to clear it.
11:8	R/W1C	0x0	CH2_ERR Task channel2 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES 1xxx: Reserved Write '1' to clear it.
7:4	R/W1C	0x0	CH1_ERR Task channel1 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES 1xxx: Reserved Write '1' to clear it.
3:0	R/W1C	0x0	CH0_ERR Task channel0 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES 1xxx: Reserved Write '1' to clear it.

4.15.5.8. Crypto Engine Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_CSAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SRC_ADR Current source address of the executing task

4.15.5.9. Crypto Engine Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_CDAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DES_ADR Current destination address of the executing task

4.15.5.10. Crypto Engine Throughput Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_TPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	THROUGHPUT It indicates the throughput of data from the whole processing. Write '0' to clear it by CPU.

4.16. Security ID

4.16.1. Overview

There is one 2Kbits on chip EFUSE, which provides 128-bit, 64-bit and one 32-bit electrical fuses for security application. The users can use them as root key, security JTAG key and other applications.

4.17. Secure Memory Controller

4.17.1. Overview

The SMC is an Advanced Microcontroller Bus Architecture compliant System-on-Chip peripheral. It is a high-performance, area-optimized address space controller with on-chip AMBA bus interfaces that conform to the AMBA Advanced Extensible Interface protocol and the AMBA Advanced Peripheral Bus protocol.

You can configure the SMC to provide the optimum security address region control functions required for your intended application.

Features:

- Enables you to program security access permissions each address region.
- Permits the transfer of data between master and slave only if the security status of the AXI transaction matches the security settings of the memory region it addresses.

4.17.2. Operations and Functional Descriptions

By default, the SMC performs read or write speculative that means it forwards an AXI transaction address to a slave, before it verifies that the AXI transaction is permitted to read address or write address respectively.

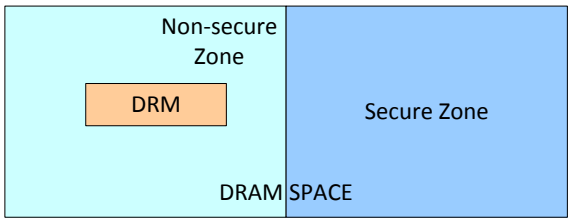
The SMC only permits the transfer of data between its AXI bus interfaces, after verified that the read or write access is permitted respectively. If the verification fails, then it prevents the transfer of data between the master and slave as denied AXI transactions.

When the speculative accesses are disabled, the SMC verifies the permissions of the access before it forwards the access to the salve. If the SMC:

- Permits the access, it commences an AXI transaction to the slave, and it adds one clock latency.
- Denies the access, it prevents the transfer of data between the master and slave. In this situation, the slave is unaware when the SMC prevents the master from accessing the slave.

4.17.2.1. DRM Block Diagram

G. NS.M stands for General Non-secure Master
D. NS.M stands for Non-secure Master appointed by DRM
S.M. stands for Secure Mater



G.NS.M only can read data from NSZ and write data into NSZ

D.NS.M can read data from NSZ and DRM, but only can write data into DRM

S.M can read data from the whole DRAM SPACE

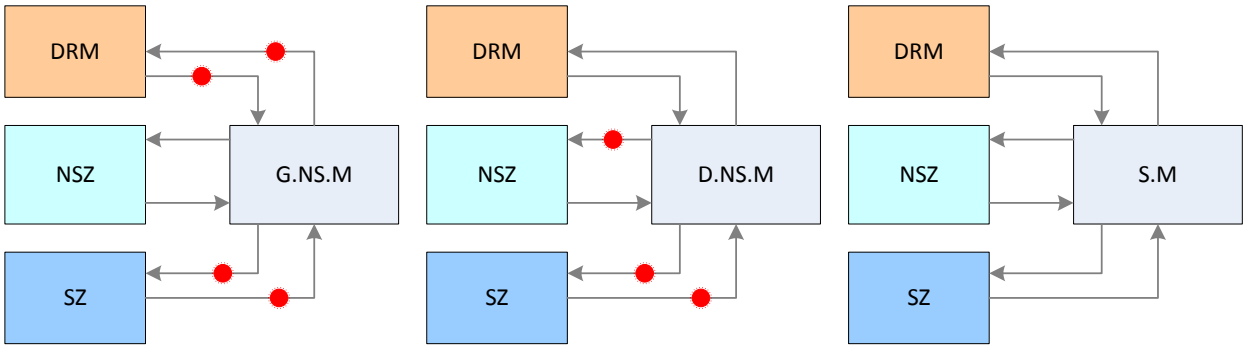


Figure 4-23. DRM Block Diagram

4.17.2.2. Master ID Table

Table 4-3. Master and Master ID

ID	Master	ID	Master
0	CPU	13	CSI
1	GPU0	14	NDFC
2	CPUS	15	Crypto Engine
3	ATH (test interface for AHB)	16	DE_RT-MIXER0
4	USB0	17	DE_RT-MIXER1
5	MSTG0 (SD/eMMC0)	18	DE_RT-WB
6	MSTG1 (SD/eMMC1)	19	
7	MSTG2 (SD/eMMC2)	20	USB3
8	USB1	21	TSC
9	USB2	22	DE Interlace
10	EMAC	23	
11	DMA	24	
12	VE	25	GPU1

4.17.2.3. Region Size Table

Table 4-4. Region Size

Size<n>	Size of Region<n>	Base Address Constraints
b000000-b001101	Reserved	-
b001110	32KB	-
b001111	64KB	Bit [15] must be zero
b010000	128KB	Bits [16:15] must be zero
b010001	256KB	Bits [17:15] must be zero
b010010	512KB	Bits [18:15] must be zero
b010011	1MB	Bits [19:15] must be zero
b010100	2MB	Bits [20:15] must be zero
b010101	4MB	Bits [21:15] must be zero
b010110	8MB	Bits [22:15] must be zero
b010111	16MB	Bits [23:15] must be zero
b011000	32MB	Bits [24:15] must be zero
b011001	64MB	Bits [25:15] must be zero
b011010	128MB	Bits [26:15] must be zero
b011011	256MB	Bits [27:15] must be zero
b011100	512MB	Bits [28:15] must be zero
b011101	1GB	Bits [29:15] must be zero
b011110	2GB	Bits [30:15] must be zero
b011111	4GB	Bits [31:15] must be zero
B100000	8GB	Bits [32:15] must be zero

4.17.2.4. Security Inversion Disabled

Table 4-5. Region Security Permissions when Security Inversion Disabled

SPN Field	Secure Read	Secure Write	Non-secure Read	Non-secure Write
4b0000	No	No	No	No
4b0100	No	Yes	No	No
4b0001, 4b0101	No	Yes	No	Yes
4b1000	Yes	No	No	No
4b0010, 4b1010	Yes	No	Yes	No
4b1100	Yes	Yes	No	No
4b1001, 4b1101	Yes	Yes	No	Yes
4b0110, 4b1110	Yes	Yes	Yes	No
4b0011-4b1111	Yes	Yes	Yes	Yes

4.17.2.5. Security Inversion Enabled

If you enable security inversion, the SMC permits you to program any combination of security permissions as Table 4-6 shows.

Table 4-6. Region Security Permissions when Security Inversion Enabled

SPN Field	Secure Read	Secure Write	Non-secure Read	Non-secure Write
4b0000	No	No	No	No
4b0001	No	No	No	Yes
4b0010	No	No	Yes	No
4b0011	No	No	Yes	Yes
4b0100	No	Yes	No	No
4b0101	No	Yes	No	Yes
4b0110	No	Yes	Yes	No
4b0111	No	Yes	Yes	Yes
4b1000	Yes	No	No	No
4b1001	Yes	No	No	Yes
4b1010	Yes	No	Yes	No
4b1011	Yes	No	Yes	Yes
4b1100	Yes	Yes	No	No
4b1101	Yes	Yes	No	Yes
4b1110	Yes	Yes	Yes	No
4b1111	Yes	Yes	Yes	Yes

4.17.3. Register List

Module Name	Base Address
SMC	0x01C1E000

Register Name	Offset	Description
SMC_CONFIG_REG	0x0000	SMC Configuration Register
SMC_ACTION_REG	0x0004	SMC Action Register
SMC_LD_RANGE_REG	0x0008	SMC Lock Down Range Register
SMC_LD_SELECT_REG	0x000C	SMC Lock Down Select Register
SMC_INT_STATUS_REG	0x0010	SMC Interrupt Status Register
SMC_INT_CLEAR_REG	0x0014	SMC Interrupt Clear Register
SMC_MST_BYP_REG	0x0018	SMC Master Bypass Register
SMC_MST_SEC_REG	0x001C	SMC Master Secure Register
SMC_FAIL_ADDR_REG	0x0020	SMC Fail Address Register
SMC_FAIL_CTRL_REG	0x0028	SMC Fail Control Register
SMC_FAIL_ID_REG	0x002C	SMC Fail ID Register
SMC_SPECU_CTRL_REG	0x0030	SMC Speculation Control Register

SMC_SEC_INV_EN_REG	0x0034	SMC Security Inversion Enable Register
SMC_MST_ATTRI_REG	0x0048	SMC Master Attribute Register
DRM_MASTER_EN_REG	0x0050	DRM Master Enable Register
DRM_ILLACCE_REG	0x0058	DRM Illegal Access Register
DRM_STATADDR_REG	0x0060	DRM Start Address Register
DRM_ENDADDR_REG	0x0068	DRM End Address Register
SMC_REGION_SETUP_LO_REG	0x0100+N*0x0010	Region Setup Low Register N (N=0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)
SMC_REGION_SETUP_HI_REG	0x0104+N*0x0010	Region Setup High Register N (N=0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)
SMC_REGION_ATTR_REG	0x0108+N*0x0010	Region Attribute Register N (N=0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)

4.17.4. Register Description

4.17.4.1. SMC Configuration Register (Default Value: 0x0000_1F0F)

Offset: 0x0000			**Register Name: SMC_CONFIG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R	0x1F	ADDR_WIDTH_RTN. Address width. Return the width of the AXI address bus. 000000~011110 : Reserved. 011111: 32-bit …… 111111: 64-bit
7:4	/	/	/
3:0	R	0xF	REGIONS_RTN. Returns the number of the regions that the SMC provides. 0000: Reserved 0001: 2 regions …… 1111: 16 regions.

4.17.4.2. SMC Action Register (Default Value: 0x0000_0001)

Offset: 0x0004			**Register Name: SMC_ACTION_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

1:0	R/W	0x1	SMC_INT_RESP. Control how the SMC uses the bresps[1:0], rresps[1:0], and smc_int signals when a region permission fails: 00: Sets smc_int LOW and issues an OKEY response 01: Sets smc_int LOW and issues a DECERR response 10: Sets smc_int HIGH and issues an OKEY response 11: Sets smc_int HIGH and issues a DECERR response

Note: This action is only valid for CPU access, not for MBUS and DMA access.

4.17.4.3. SMC Lockdown Range Register (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: SMC_LD_RANGE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LOCKDOWN_EN. When setting to 1, it enables the lockdown_regions field to control the regions that are to be locked.
30:4	/	/	/
3:0	R/W	0x0	NO_REGIONS_LOCKDOWN. Control the number of regions to lockdown when the enable bit is set to 1. 0000: region no_of_regions-1 is locked 0001: region no_of_regions-1 to region no_of_regions-2 are locked …… 1111: region no_of_regions-1 to region no_of_regions-16 are locked

Note: No_of_regions is the value of the no_of_regions field in the configuration register.
The value programmed in the **SMC_LD_RANGE_REG** register must not be greater than no_of_regions-1 ,else all regions are locked.

4.17.4.4. SMC Lockdown Select Register (Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: SMC_LD_SELECT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ACCESS_TYPE_SPECU. Modify the access type of the **SMC_SPECU_CTRL_REG** register. 0: No effect. The **SMC_SPECU_CTRL_REG** register remains RW. 1:The **SMC_SPECU_CTRL_REG** register is RO.
1	R/W	0x0	ACCESS_TYPE_SEC_INV_EN. Modify the access type of the **SMC_SEC_INV_EN_REG** register. 0: No effect. The **SMC_SEC_INV_EN_REG** register remains RW.

			1:The **SMC_SEC_INV_EN_REG** register is RO.
0	R/W	0x0	ACCESS_TYPE_LOCKDOWN_RANGE. Modify the access type of the **SMC_LD_RANGE_REG** register. 0: No effect. The **SMC_LD_RANGE_REG** register remains RW. 1: The **SMC_LD_RANGE_REG** register is RO.

4.17.4.5. SMC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: SMC_INT_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R	0x0	INT_OVERRUN. When setting to 1, it indicates the occurrence of two or more region permission failure since the interrupt was last cleared.
0	R	0x0	INT_STATUS. Return the status of the interrupt. 0: Interrupt is inactive. 1: Interrupt is active.

4.17.4.6. SMC Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: SMC_INT_CLEAR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SMC_CLR_REG. Write any value to the int_clear register sets the : Status bit to 0 in the int_status register Overrun bit to 0 in the int_status register. **Note:** It will be automatically cleared after the write operation.

4.17.4.7. SMC Master Bypass Register (Default Value: 0xFFFF_FFFF)

Offset: 0x0018			**Register Name: SMC_MST_BYP_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	SMC_MASTER_BYPASS_EN. SMC Master n Bypass Enable. (n = 0~31, see the **Master and Master ID** in Table 4-3 for detail.) 0: Bypass Disable 1: Bypass Enable.

			Note: Bit[31:0] stand for Master ID [31:0]. If the master n bypass enable is set to 0, the master n access must be through the SMC.

4.17.4.8. SMC Master Secure Register (Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SMC_MST_SEC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SMC_MASTER_SEC. SMC Master n Secure Configuration.(n = 0~31, see the **Master and Master ID** in Table 4-3 for detail) 0: Secure 1: Non-secure.

4.17.4.9. SMC Fail Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: SMC_FAIL_ADDR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	FIRST_ACCESS_FAIL. Return the address bits [31:0] of the first access to fail a region permission check after the interrupt was cleared. For external 16-bit DDR2, the address [2:0] is fixed to zero. For external 32-bit DDR2 and 16-bit DDR3, the address [3:0] is fixed to zero. For external 32-bit DDR3, the address [4:0] is fixed to zero.

Note: If the master ID="SRAM" and the register value is between 0x80000 to 0xBFFFF, the real address should be divided by 4.

4.17.4.10. SMC Fail Control Register (Default Value: 0x0000_0000)

Offset: 0x0028			**Register Name: SMC_FAIL_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	READ_WRITE. This bit indicates whether the first access to fail a region permission check was a write or read as: 0: Read access 1: Write access.
23:22	/	/	/
21	R	0x0	NON_SECURE. After cleared the interrupt status, this bit indicates whether the first access

			to fail a region permission check was non-secure. Read as: 0: Secure access 1: Non-secure access
20	R	0x0	PRIVILEGED. After clearing the interrupt status, this bit indicates whether the first access to fail a region permission check was privileged. Read as: 0: Unprivileged access. 1: Privileged access
19:0	/	/	/

4.17.4.11. SMC Fail ID Register (Default Value: 0x0000_1F00)

Offset: 0x002C			Register Name: SMC_FAIL_ID_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R	0x0	FAIL_BST_LEN. Fail burst length. 00000000: 1 word length …… 00001111: 16 words length
15:8	/	/	/
7:0	R	0x0	FAIL_MASTER_ID. Fail Master ID. The value stands for master id, see the **Master and Master ID** in Table 4-3 for detail.

4.17.4.12. SMC Speculation Control Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMC_SPECU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	WRITE_SPECU. Write_speculation. Control the write access speculation. 0: Write access speculation is enabled 1: Write access speculation is disabled.
0	R/W	0x0	READ_SPECU. Read_speculation. Control the read access speculation.

			0: Read access speculation is enabled 1: Read access speculation is disabled.

4.17.4.13. SMC Security Inversion Enable Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMC_SEC_INV_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	SEC_INV_EN. Security_inversion_en. Controls whether the SMC permits security inversion to occur. 0: security inversion is not permitted. 1: security inversion is permitted. This enables a region to be accessible to masters in non-secure state but not accessible to masters in secure state. See **Region Security Permissions when Security Inversion Disabled** in Table 4-5 and **Region Security Permissions when Security Inversion Enabled** in Table 4-6.

4.17.4.14. SMC Master Attribute Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMC_MST_ATTRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MST_ATTRI. 0: The secure attribute of master is up to master security extensions. 1: The secure attribute of master is up to **SMC Master Secure Register**.

4.17.4.15. DRM Master Enable Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: DRM_MASTER_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DRM_EN. DRM enable.
30:12	/	/	/
13	R/W	0x0	GPU_WRITE_EN GPU write enable
12	R/W	0x0	GPU_READ_EN GPU read enable
11:8	/	/	/
7	R/W	0x0	DE_INTERLACE

			DE_ INTERLACE enable
6	R/W	0x0	DE_RT-WB DE_RT-WB enable
5	R/W	0x0	DE_RT-MIXER1 DE_RT-MIXER1 enable
4	R/W	0x0	DE_RT-MIXER0 DE_RT-MIXER0 enable
3:1	/	/	/
0	R/W	0x0	VE_ENCODE_EN VE encode enable

4.17.4.16. DRM Illegal Access Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: DRM_ILLACCE_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DRM_ILLACCE_REG. When a master, which is non-secure, accesses the DRM space, then the relevant bit will be set up. See **Master and Master ID** in Table 4-3 for detail.

4.17.4.17. DRM Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: DRM_STATADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	R/W	0x0	DRM_STATADDR_REG.
14:0	/	/	/

4.17.4.18. DRM End Address Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: DRM_ENDADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	R/W	0x0	DRM_ENDADDR_REG.
14:0	/	/	/

4.17.4.19. SMC Region Setup Low Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0010(N=0~15)			Register Name: SMC_REGION_SETUP_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	R/W	0x0	BASE_ADDRESS_LOW. Controls the base address [31:15] of region<n>. The SMC only permits a region to start at address 0x0, or at a multiple of its region size. For example, if the size of a region is 512MB, and it is not at

			address 0x0, the only valid settings for this field are: 17'b00100000000000000 17'b01000000000000000 17'b01100000000000000 17'b10000000000000000 17'b10100000000000000 17'b11000000000000000 17'b11100000000000000
14:0	/	/	/

Note: For region 0, this field is Read Only (RO). The SMC sets the base address of region 0 to 0x0.
The base address should be equal to the DRAM absolute address.

4.17.4.20. SMC Region Setup High Register (Default Value: 0x0000_0000)

Offset: 0x0104+N*0x0010(N=0~15)			Register Name: SMC_REGION_SETUP_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BASE_ADDRESS_HIGH The SMC only permits a region to start at address 0x0, or at a multiple of its region size. If you program a region size to be 8GB or more, then the SMC might ignore certain bits depending on the region size.

4.17.4.21. SMC Region Attributes Register (Default Value: 0x0000_0000)

Offset: 0x0108+N*0x0010(N=0~15)			Register Name: SMC_REGION_ATTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	REGION_ATTR_SPN. SP<n>. Permission setting for region <n>. If an AXI transaction occurs to region n, the value in the sp<n> field controls whether the SMC permits the transaction to proceed. See **Region Security Permissions when Security Inversion Disabled** in Table 4-5 and **Region Security Permissions when Security Inversion Enabled** in Table 4-6.
27:16	/	/	/.
15:8	R/W	0x0	SUB_REGION_DISABLE. Subregion_disable. Regions are split into eight equal-size sub-regions, and each bit enables the corresponding subregion to be disabled. Bit [15] = 1 subregion 7 is disabled. Bit [14] = 1 subregion 6 is disabled. Bit [13] = 1 subregion 5 is disabled. Bit [12] = 1 subregion 4 is disabled. Bit [11] = 1 subregion 3 is disabled.

			Bit [10] = 1 subregion 2 is disabled. Bit [9] = 1 subregion 1 is disabled. Bit [8] = 1 subregion 0 is disabled.
7	/	/	/
6:1	R/W	0x0	REGION_ATTR_SIZE. Size<n>. Size of region<n>, see **Region Size** in Table 4- 4 for detail.
0	R/W	0x0	REGION_ATTR_EN. EN<n>. Enable for region<n>. 0: Region < n> is disabled. 1: Region < n> is enabled.

Note: For region 0, this field is reserved except SPN field.

4.18. Secure Peripherals Controller

4.18.1. Overview

The Secure Peripherals Controller(SPC) provides a software interface to the protection bits in a secure system of a TrustZone design. It provides system flexibility that enables to configure different areas of memory as secure or non-secure.

Features:

- It has protection bits to program some areas of memory as secure or non–secure.

4.18.2. Operations and Functional Descriptions

4.18.2.1. Typical Applications

The SPC provides a software interface to set up memory areas as secure or non-secure. There are two ways:

- Programmable protection bits that can be allocated to areas of memory as determined by an external decoder
- Programmable region size value for use by an AXI TrustZone Memory Adapter.

4.18.2.2. SPC Configuration Table

The following table shows the configuration region of SPC.

Table 4-7. SPC Configuration Table

Register	Bit	SPC0	SPC1	SPC2
		Module Name	Module Name	Module Name
SPC DECPORTx (x=0,1,2)	[0]	/	NAND	VE SRAM
	[1]	TWI0	DMA	R_CPUCFG
	[2]	TWI1	Crypto Engine	System Control
	[3]	SPI0	SRAM A1	CCU
	[4]	SPI1	USB_OTG_Device	DE
	[5]	GPIO	USB Host0	RTC
	[6]	CPU_CFG	DRAMC	R_INTC
	[7]	SMHC0	PRCM	

4.18.3. Register List

Module Name	Base Address
SPC	0x01C23400

Register Name	Offset	Description
SPC_DECPORT0_STA_REG	0x0004	SPC Decode Port0 Status Register
SPC_DECPORT0_SET_REG	0x0008	SPC Decode Port0 Set Register
SPC_DECPORT0_CLR_REG	0x000C	SPC Decode Port0 Clear Register
SPC_DECPORT1_STA_REG	0x0010	SPC Decode Port1 Status Register
SPC_DECPORT1_SET_REG	0x0014	SPC Decode Port1 Set Register
SPC_DECPORT1_CLR_REG	0x0018	SPC Decode Port1 Clear Register
SPC_DECPORT2_STA_REG	0x001C	SPC Decode Port2 Status Register
SPC_DECPORT2_SET_REG	0x0020	SPC Decode Port2 Set Register
SPC_DECPORT2_CLR_REG	0x0024	SPC Decode Port2 Clear Register

4.18.4. Register Description

4.18.4.1. SPC DECPORT0 Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SPC_DECPORT0_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	STA_DEC_PROT0_OUT. Shows the status of the decode protection output 0: Decode region corresponding to the bit is secure 1: Decode region corresponding to the bit is non-secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.2. SPC DECPORT0 Set Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: SPC_DECPORT0_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7:0	W	0x0	SET_DEC_PORT0_OUT. Sets the corresponding decode protection output. 0: No effect

			1: Set decode region to non-secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.3. SPC DECPORT0 Clear Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SPC_DECPORT0_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	CLR_DEC_PROT0_OUT. Clears the corresponding decode protection output. 0: No effect 1: Set decode region to secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.4. SPC DECPORT1 Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPC_DECPORT1_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	STA_DEC_PROT1_OUT. Shows the status of the decode protection output. 0: Decode region corresponding to the bit is secure 1: Decode region corresponding to the bit is non-secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.5. SPC DECPORT1 Set Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: SPC_DECPORT1_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	SET_DEC_PORT1_OUT. Sets the corresponding decode protection output. 0: No effect

			1: Set decode region to non-secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.6. SPC DECPORT1 Clear Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SPC_DECPORT1_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	CLR_DEC_PROT1_OUT. Clears the corresponding decode protection output. 0: No effect 1: Set decode region to secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.7. SPC DECPORT2 Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPC_DECPORT2_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	STA_DEC_PROT2_OUT. Show the status of the decode protection output. 0: Decode region corresponding to the bit is secure 1: Decode region corresponding to the bit is non-secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.8. SPC DECPORT2 Set Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPC_DECPORT2_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	SET_DEC_PORT2_OUT. Sets the corresponding decode protection output. 0: No effect

			1: Set decode region to non-secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.18.4.9. SPC DECPORT2 Clear Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SPC_DECPORT2_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	CLR_DEC_PROT2_OUT. Clears the corresponding decode protection output. 0: No effect 1: Set decode region to secure. There is one bit of the register for each protection output (See the **SPC Configuration Table** in Table 4-7 for detail).

4.19. Thermal Sensor Controller

4.19.1. Overview

Thermal sensors have become common elements in wide range of modern system on chip (SOC) platform. Thermal sensors are used to constantly monitor the temperature on the chip.

The Thermal Sensor Controller embeds two thermal sensors, sensor0 for CPU,sensor1 for GPU .Thermal sensors can generate interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

Features:

- Supports APB 32-bit bus width
- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Power supply voltage:3.3V
- Low power dissipation
- Periodic temperature measurement
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

4.19.2. Block Diagram

Figure 4-24 shows a block diagram of the Thermal Sensor.

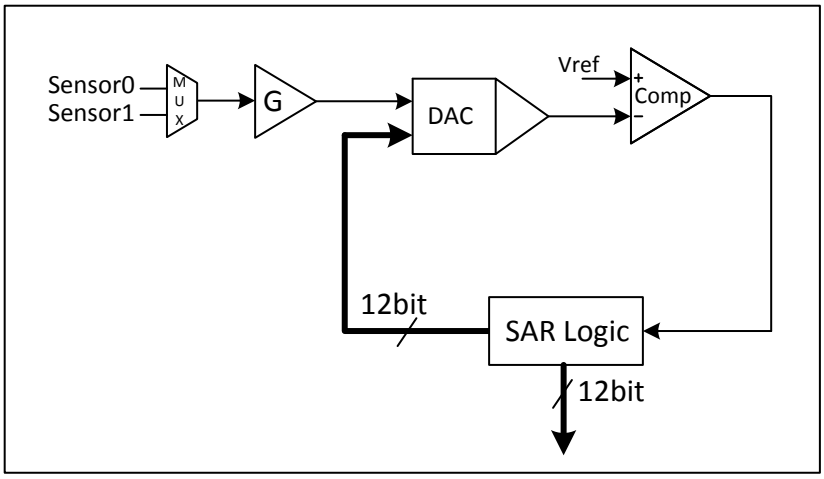


Figure 4-24. Thermal Sensor Block Diagram

4.19.3. Clock and Timing Requirements

CLK_IN = 24MHz/M, M can be set in the CCU

Conversion Time = 1/(24MHz/M/14Cycles) =0.583 * M (us)

THERMAL_PER (configured by the value of THERMAL_PER) is must be greater than (ACQ1 + ACQ0+Conversion Time)

THERMAL_PER > ACQ1 + ACQ0 + Conversion Time

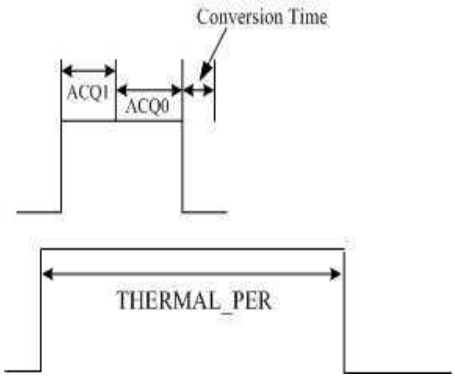


Figure 4-25. Thermal Conversion Phase

4.19.4. Programming Guidelines

1) Timing must be like this: THERMAL_PER > ACQ1 + ACQ0 + Conversion Time
2) Configure the **THS Interrupt Control Register** to set the THERMAL_PER and IRQ
3) Configure the **Alarm Threshold Control Register** and **Shutdown Threshold Control Register** to set the **ALARM0_T_HOT** and **SHUT0_T_HOT**
4) Configure the **THS Control Register0** to set the **SENSOR_ACQ0** and enable the sensor
5) THS temperature formula:

   When temperature is lower than 70℃ (**THS0_DATA** or **THS1_DATA** is higher than 0x500) , then

   Tem_THS0 = -0.1191 * **THS0_DATA** + 223, Tem_THS1 = -0.1191 * **THS1_DATA** +223

   When temperature is higher than 70℃ (**THS0_DATA** or **THS1_DATA** is lower than 0x500) , then

   Tem_THS0 = -0.1452 * **THS0_DATA** + 259, Tem_THS1 = -0.159 * **THS1_DATA** + 276

4.19.5. Register List

Module Name	Base Address
Thermal Sensor	0x01C25000

Register Name	Offset	Description
THS_CTRL0	0x0000	THS Control Register0
THS_CTRL2	0x0040	THS Control Register2
THS_INT_CTRL	0x0044	THS Interrupt Control Register
THS_STAT	0x0048	THS Status Register

THS0_ALARM_CTRL	0x0050	Alarm Threshold Control Register0
THS1_ALARM_CTRL	0x0054	Alarm Threshold Control Register1
THS0_SHUTDOWN_CTRL	0x0060	Shutdown Threshold Control Register0
THS1_SHUTDOWN_CTRL	0x0064	Shutdown Threshold Control Register1
THS_FILTER	0x0070	Average Filter Control Register
THS_CDATA	0x0074	Thermal Sensor Calibration Data
THS0_DATA	0x0080	THS Data Register0
THS1_DATA	0x0084	THS Data Register1

4.19.6. Register Description

4.19.6.1. THS Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: THS_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	SENSOR_ACQ Sensor acquire time CLK_IN/(N+1)

4.19.6.2. THS Control Register2 (Default Value: 0x0004_0000)

Offset: 0x0040			Register Name: THS_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x4	ADC_ACQ. ADC acquire time CLK_IN/(N+1)
15:3	/	/	/
2	/	/	/
1	R/W	0x0	SENSE1_EN. Enable temperature measurement of sensor1 0:Disable 1:Enable
0	R/W	0x0	SENSE0_EN. Enable temperature measurement of sensor0 0:Disable 1:Enable

4.19.6.3. THS Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: THS_INT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	THERMAL_PER. 4096*(n+1)/CLK_IN
11	/	/	/
10	/	/	/
9	R/W	0x0	THS1_DATA_IRQ_EN. Enable temperature measurement data of sensor1 0: Disable 1: Enable
8	R/W	0x0	THS0_DATA_IRQ_EN. Enable temperature measurement data of sensor0 0: Disable 1: Enable
7	/	/	/
6	/	/	/
5	R/W	0x0	SHUT_INT1_EN. Enable shutdown interrupt of sensor1 0: Disable 1: Enable
4	R/W	0x0	SHUT0_INT_EN. Enable shutdown interrupt of sensor0 0: Disable 1: Enable
3	/	/	/
2	/	/	/
1	R/W	0x0	ALARM_INT1_EN. Enable alarm interrupt of sensor1 0: Disable 1: Enable
0	R/W	0x0	ALARM_INT0_EN. Enable alarm interrupt of sensor0 0: Disable 1: Enable

4.19.6.4. THS Status Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: THS_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	/	/	/
13	R/W1C	0x0	ALARM1_OFF_STS. Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
12	R/W1C	0x0	ALARM0_OFF_STS. Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
11	/	/	/
10	/	/	/
9	R/W1C	0x0	THS1_DATA_IRQ_STS. Data interrupt status for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
8	R/W1C	0x0	THS0_DATA_IRQ_STS. Data interrupt status for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
7:6	/	/	/
5			
4	R/W1C	0x0	THS1_SHUT_INT_STS. Shutdown interrupt status for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
3	R/W1C	0x0	THS0_SHUT_INT_STS. Shutdown interrupt status for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
2	/	/	/
1	R/W1C	0x0	THS1_ALARM_INT_STS. Alarm interrupt pending for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails
0	R/W1C	0x0	THS0_ALARM_INT_STS. Alarm interrupt pending for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails

4.19.6.5. Alarm Threshold Control Register0 (Default Value: 0x05A0_0684)

Offset: 0x0050			Register Name: THS0_ALARM_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT. Thermal sensor0 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal sensor0 alarm threshold for hysteresis temperature

Note: When Tem_THS0 is above **ALARM0_T_HOT**, THS0 alarm hot IRQ will generate. When Tem_THS0 is less than **ALARM0_T_HYST**, THS0 alarm hysteresis IRQ will generate.

4.19.6.6. Alarm Threshold Control Register1 (Default Value: 0x05A0_0684)

Offset: 0x0054			Register Name: THS1_ALARM_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT. Thermal sensor1 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal sensor1 alarm threshold for hysteresis temperature

Note: When Tem_THS1 is above **ALARM1_T_HOT**, THS1 alarm hot IRQ will generate. When Tem_THS1 is less than **ALARM1_T_HYST**, THS1 alarm hysteresis IRQ will generate.

4.19.6.7. Shutdown Threshold Control Register0 (Default Value: 0x04E9_0000)

Offset: 0x0060			Register Name: THS0_SHUTDOWN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT0_T_HOT. Thermal sensor0 shutdown threshold for hot temperature
15:0	/	/	/

Note: When Tem_THS0 is above **SHUT0_T_HOT**, THS0 shutdown IRQ will generate.

4.19.6.8. Shutdown Threshold Control Register1 (Default Value: 0x04E9_0000)

Offset: 0x0064			Register Name: THS1_SHUTDOWN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT.

			Thermal sensor1 shutdown threshold for hot temperature
15:0	/	/	/

Note: When Tem_THS1 is above **SHUT1_T_HOT**, THS1 shutdown IRQ will generate.

4.19.6.9. Average Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0070			Register Name: THS_FILTER _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Average Filter Type 00: 2 01: 4 10: 8 11: 16

4.19.6.10. Thermal Sensor Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x0074			Register Name: THS_CDATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x800	THS1_CDATA. Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA. Thermal Sensor0 calibration data

4.19.6.11. THS0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: THS0_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA. Temperature measurement data of sensor0

4.19.6.12. THS1 Data Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: THS1_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA. Temperature measurement data of sensor1

4.20. KEYADC

4.20.1. Overview

KEYADC is 6-bit resolution ADC for key application. The KEYADC can work up to 250Hz conversion rate.

Features:

- Up to 6-bit resolution
- Sample rate up to 250Hz
- Supports APB 32-bit bus width,reference voltage is 2.2V
- Supports interrupt
- Supports general key, hold key and already hold key
- Supports normal, single and continue work mode
- Voltage input range between 0V to 2.2V

4.20.2. Block Diagram

Figure 4-26 shows the block diagram of the KEYADC.

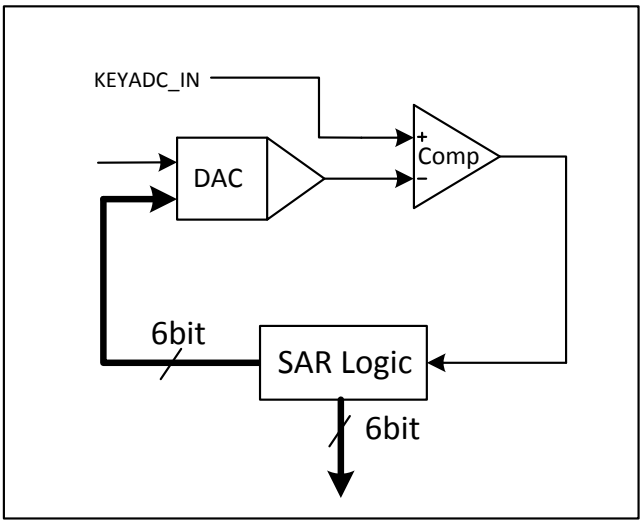


Figure 4-26. KEYADC Block Diagram

4.20.3. Operations and Functional Descriptions

4.20.3.1. External Signals

Table 4-8 describes the external signals of KEYADC. KEYADC pin is the analog input signal.

Table 4-8. KEYADC External Signals

Signal	Description	Type
KEYADC	ADC channel for key application	AI

4.20.3.2. Clock Sources

KEYADC has one clock source. Table 4-9 describes the clock source for KEYADC.

Table 4-9. KEYADC Clock Sources

Clock Sources	Description
LOSC	32KHz Clock

4.20.3.3. KEYADC Work Mode

(1).Normal Mode

ADC gathers 8 samples,the average of the 8 samples is updated in data register,and the data interrupt sign is enabled.It is sampled repeatedly according to this mode until ADC stop.

(2).Continue Mode

ADC gathers 8 samples every other 8*(N+1) sample cycle. The average of every 8 samples is updated in the data register, and the data interrupt sign is enabled. (N is defined in the bit[19:16] of **KEYADC_CTRL_REG**).

(3).Single Mode

ADC gathers 8 samples, the average of the 8 samples is updated in data register, and the data interrupt sign is enabled, since then ADC stops sample.

4.20.3.4. KEYADC Operation Principle

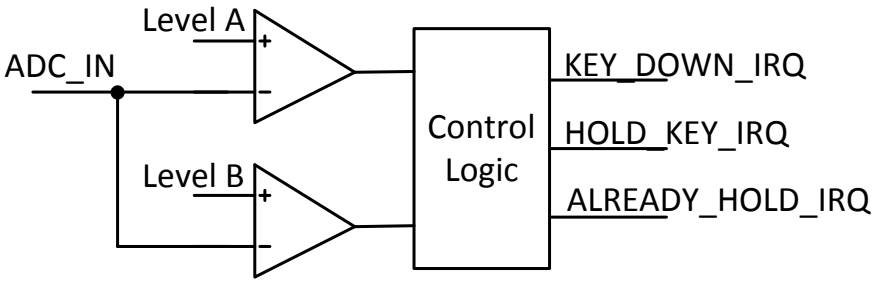


Figure 4-27. KEYADC Converted Data Diagram

Level A: 2.0V

Level B: Configurable by **LEVELB_VOL**

When ADC_IN signal is less than Level A and Level B, the key down interrupt will generate. When ADC_IN signal is only less than Level A, the hold key interrupt will generate. When ADC_IN signal is only less than Level B, the already hold key interrupt will generate.

If ADC_IN signal is less than Level A, and in a certain time range (configurable by **LEVEL_A_B_CNT**) ADC_IN signal is not less than Level B, the hold key interrupt will generate. If ADC_IN signal is less than Level A , and in a certain time range (configurable by **LEVEL_A_B_CNT**) ADC_IN signal is less than Level B, the key down interrupt will generate . If ADC_IN signal is less than Level B, and ADC_IN signal is not less than Level A, the already hold key interrupt will generate.

The KEYADC have three modes, **Normal Mode**、**Single Mode** and **Continue Mode**. **Normal Mode** is that the KEYADC will report the converted result data all the time when the key is down. **Single Mode** is that the KEYADC will only report the first converted result data when the key is down. **Continue Mode** is that the KEYADC will report the converted result data every other 8*(N+1) sample when key is down.

The KEYADC supports four sample rate such as 250 Hz、125 Hz、62.5 Hz and 32.25 Hz, you can configure the value of **KEYADC_SAMPLE_RATE** to select the fit sample rate.

4.20.4. Programming Guidelines

(1).The input voltage need be controlled in the range from 0 to **LEVELB_VOL** (**LEVELB_VOL** is defined in the bit[5:4] of **KEYADC_CTRL_REG**).

(2).KEYADC_DATA = Vin/V_{REF}*63 (V_{REF}=2.2V).

4.20.5. Register List

Module Name	Base Address
KEYADC	0x01C21800

Register Name	Offset	Description
KEYADC_CTRL	0x0000	KEYADC Control Register
KEYADC_INTC	0x0004	KEYADC Interrupt Control Register
KEYADC_INTS	0x0008	KEYADC Interrupt Status Register
KEYADC_DATA	0x000C	KEYADC Data Register

4.20.6. Register Description

4.20.6.1. KEYADC Control Register (Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: KEYADC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 24	R/W	0x1	FIRST_CONVERT_DLY. ADC First Convert Delay Setting ADC conversion is delayed by n samples
23:22	R/W	0x0	Reserved to 0
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode Time Select One of 8*(N+1) sample as a valuable sample data
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples
7	R/W	0x0	KEYADC_HOLD_KEY_EN KEYADC Hold Key Enable 0: Disable 1: Enable
6	R/W	0x1	KEYADC_HOLD_EN. KEYADC Sample Hold Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (~2.1V) 01: 0x39 (~1.99V) 10: 0x36 (~1.86V) 11: 0x33 (~1.78V)
3: 2	R/W	0x2	KEYADC_SAMPLE_RATE. KEYADC Sample Rate

			00: 250 Hz 01: 125 Hz 10: 62.5 Hz 11: 32.25 Hz
1	/	/	/
0	R/W	0x0	KEYADC_EN. KEYADC Enable 0: Disable 1: Enable

4.20.6.2. KEYADC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: KEYADC_INTC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	ADC_KEYUP_IRQ_EN. ADC Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC_ALRDY_HOLD_IRQ_EN. ADC Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC_HOLD_IRQ_EN. ADC Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC_KEYDOWN_EN ADC Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC_DATA_IRQ_EN. ADC Data IRQ Enable 0: Disable 1: Enable

4.20.6.3. KEYADC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name:KEYADC_INTS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	ADC_KEYUP_PENDING. ADC Key Up Pending Bit When the general key pull up, the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W1C	0x0	ADC_ALRDY_HOLD_PENDING. ADC Already Hold Pending Bit When hold key is in the pull-down state, at this time the general key is pulled down, then the **ADC_ALRDY_HOLD_PENDING** bit is set 1 by hardware if the **ADC_ALRDY_HOLD_IRQ_EN** bit is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC_HOLDKEY_PENDING. ADC Hold Key Pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W1C	0x0	ADC_KEYDOWN_PENDING. ADC Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

0	R/W1C	0x0	ADC_DATA_PENDING. ADC Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

4.20.6.4. KEYADC Data Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: KEYADC_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x0	KEYADC_DATA. KEYADC Data

4.21. Port Controller(CPUx-PORT)

4.21.1. Overview

The chip has 7 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 22 input/output port
- Port C(PC): 17 input/output port
- Port D(PD): 18 input/output port
- Port E(PE) : 16 input/output port
- Port F(PF) : 7 input/output port
- Port G(PG) : 14 input/output port
- Port L(PL) : 12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions are not used. The total 3 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

4.21.2. Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	0x0000 + n*0x24	Port n Configure Register 0 (n from 0 to 6)
Pn_CFG1	0x0004 + n*0x24	Port n Configure Register 1 (n from 0 to 6)
Pn_CFG2	0x0008 + n*0x24	Port n Configure Register 2 (n from 0 to 6)
Pn_CFG3	0x000C + n*0x24	Port n Configure Register 3 (n from 0 to 6)
Pn_DAT	0x0010 + n*0x24	Port n Data Register (n from 0 to 6)
Pn_DRV0	0x0014 + n*0x24	Port n Multi-Driving Register 0 (n from 0 to 6)
Pn_DRV1	0x0018 + n*0x24	Port n Multi-Driving Register 1 (n from 0 to 6)
Pn_PUL0	0x001C + n*0x24	Port n Pull Register 0 (n from 0 to 6)
Pn_PUL1	0x0020 + n*0x24	Port n Pull Register 1 (n from 0 to 6)
PA_INT_CFG0	0x0200 + 0x00 + 0*0x20	PIO Interrrupt Configure Register 0
PA _INT_CFG1	0x0200 + 0x04 + 0*0x20	PIO Interrrupt Configure Register 1
PA _INT_CFG2	0x0200 + 0x08 + 0*0x20	PIO Interrrupt Configure Register 2
PA _INT_CFG3	0x0200 + 0x0C + 0*0x20	PIO Interrrupt Configure Register 3
PA _INT_CTL	0x0200 + 0x10 + 0*0x20	PIO Interrupt Control Register
PA _INT_STA	0x0200 + 0x14 + 0*0x20	PIO Interrupt Status Register
PA_INT_DEB	0x0200 + 0x18 + 0*0x20	PIO Interrupt Debounce Register
PF_INT_CFG0	0x0200 + 0x00 + 1*0x20	PIO Interrrupt Configure Register 0

PF_INT_CFG1	0x0200 + 0x04 + 1*0x20	PIO Interrrupt Configure Register 1
PF_INT_CFG2	0x0200 + 0x08 + 1*0x20	PIO Interrrupt Configure Register 2
PF_INT_CFG3	0x0200 + 0x0C + 1*0x20	PIO Interrrupt Configure Register 3
PF_INT_CTL	0x0200 + 0x10 + 1*0x20	PIO Interrupt Control Register
PF_INT_STA	0x0200 + 0x14 + 1*0x20	PIO Interrupt Status Register
PF_INT_DEB	0x0200 + 0x18 + 1*0x20	PIO Interrupt Debounce Register
PG_INT_CFG0	0x0200 + 0x00 + 2*0x20	PIO Interrrupt Configure Register 0
PG _INT_CFG1	0x0200 + 0x04 + 2*0x20	PIO Interrrupt Configure Register 1
PG _INT_CFG2	0x0200 + 0x08 + 2*0x20	PIO Interrrupt Configure Register 2
PG _INT_CFG3	0x0200 + 0x0C + 2*0x20	PIO Interrrupt Configure Register 3
PG _INT_CTL	0x0200 + 0x10 + 2*0x20	PIO Interrupt Control Register
PG _INT_STA	0x0200 + 0x14 + 2*0x20	PIO Interrupt Status Register
PG _INT_DEB	0x0200 + 0x18 + 2*0x20	PIO Interrupt Debounce Register

4.21.3. Register Description

4.21.3.1. PA Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000			**Register Name: PA_CFG0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PA7_SELECT 000:Input 001:Output 010:SIM0_CLK 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PA6_SELECT 000:Input 001:Output 010:SIM0_PWREN 011:PCM0_MCLK 100:Reserved 101:Reserved 110:PA_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PA5_SELECT 000:Input 001:Output 010:UART0_RX 011:PWM0 100:Reserved 101:Reserved 110:PA_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PA4_SELECT

			000:Input 001:Output 010:UART0_TX 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PA3_SELECT 000:Input 001:Output 010:UART2_CTS 011:JTAG_DI 100:Reserved 101:Reserved 110:PA_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA2_SELECT 000:Input 001:Output 010:UART2_RTS 011:JTAG_DO 100:Reserved 101:Reserved 110:PA_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PA1_SELECT 000:Input 001:Output 010:UART2_RX 011:JTAG_CK 100:Reserved 101:Reserved 110:PA_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PA0_SELECT 000:Input 001:Output 010:UART2_TX 011:JTAG_MS 100:Reserved 101:Reserved 110:PA_EINT0 111:IO Disable

4.21.3.2. PA Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0004			Register Name: PA_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PA15_SELECT 000:Input 001:Output 010:SPI1_MOSI 011:UART3_RTS 100:Reserved 101:Reserved

			110:PA_EINT15 111:IO Disable
27	/	/	
26:24	R/W	0x7	PA14_SELECT 000:Input 001:Output 010:SPI1_CLK 011:UART3_RX 100:Reserved 101:Reserved 110:PA_EINT14 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PA13_SELECT 000:Input 001:Output 010:SPI1_CS 011:UART3_TX 100:Reserved 101:Reserved 110:PA_EINT13 111:IO Disable
19	/	/	
18:16	R/W	0x7	PA12_SELECT 000:Input 001:Output 010:TWI0_SDA 011:DI_RX 100:Reserved 101:Reserved 110:PA_EINT12 111:IO Disable
15	/	/	
14:12	R/W	0x7	PA11_SELECT 000:Input 001:Output 010:TWI0_SCK 011:DI_TX 100:Reserved 101:Reserved 110:PA_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA10_SELECT 000:Input 001:Output 010:SIM0_DET 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT10 111:IO Disable
7	/	/	
6:4	R/W	0x7	PA9_SELECT 000:Input 001:Output 010:SIM0_RST 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT9 111:IO Disable
3	/	/	
2:0	R/W	0x7	PA8_SELECT

			000:Input 001:Output 010:SIM0_DATA 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT8 111:IO Disable

4.21.3.3. PA Configure Register 2 (Default Value: 0x0077_7777)

Offset: 0x0008			Register Name: PA_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	
22:20	R/W	0x7	PA21_SELECT 000:Input 001:Output 010:PCM0_DIN 011:SIM0_VPPPP 100:Reserved 101:Reserved 110:PA_EINT21 111:IO Disable
19	/	/	
18:16	R/W	0x7	PA20_SELECT 000:Input 001:Output 010:PCM0_DOUT 011:SIM0_VPPEN 100:Reserved 101:Reserved 110:PA_EINT20 111:IO Disable
15	/	/	
14:12	R/W	0x7	PA19_SELECT 000:Input 001:Output 010:PCM0_CLK 011:TWI1_SDA 100:Reserved 101:Reserved 110:PA_EINT19 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PA18_SELECT 000:Input 001:Output 010:PCM0_SYNC 011:TWI1_SCK 100:Reserved 101:Reserved 110:PA_EINT18 111:IO Disable
7	/	/	
6:4	R/W	0x7	PA17_SELECT 000:Input 001:Output 010:OWA_OUT 011:Reserved 100:Reserved 101:Reserved 110:PA_EINT17 111:IO Disable

3	/	/	
2:0	R/W	0x7	PA16_SELECT 000:Input 001:Output 010:SPI1_MISO 011:UART3_CTS 100:Reserved 101:Reserved 110:PA_EINT16 111:IO Disable

4.21.3.4. PA Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PA_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.5. PA Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PA_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	0x0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.6. PA Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0014			Register Name: PA_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.7. PA Multi-Driving Register 1 (Default Value: 0x0000_0555)

Offset: 0x0018			Register Name: PA_DRV1 _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i]	R/W	0x1	PA_DRV

(i=0~5)			PA[n] Multi-Driving Select (n = 16~21) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.8. PA PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PA_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.9. PA PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PA_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~21) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.10. PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000:Input 001:Output 010:NAND_RB1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC6_SELECT

			000:Input 001:Output 010:NAND_RB0 011:SDC2_CMD 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC5_SELECT 000:Input 001:Output 010:NAND_RE 011:SDC2_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC4_SELECT 000:Input 001:Output 010:NAND_CE0 011:Reserved 100:SPI0_MISO 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PC3_SELECT 000:Input 001:Output 010:NAND_CE1 011:SPI0_CS 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PC2_SELECT 000:Input 001:Output 010:NAND_CLE 011:SPI0_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PC1_SELECT 000:Input 001:Output 010:NAND_ALE 011:SPI0_MISO 100:SDC2_DS 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/

2:0	R/W	0x7	PC0_SELECT 000:Input 001:Output 010:NAND_WE 011:SPI0_MOSI 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.11. PC Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x004C			Register Name: PC_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC15_SELECT 000:Input 001:Output 010:NAND_DQ7 011:SDC2_D7 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PC14_SELECT 000:Input 001:Output 010:NAND_DQ6 011:SDC2_D6 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PC13_SELECT 000:Input 001:Output 010:NAND_DQ5 011:SDC2_D5 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC12_SELECT 000:Input 001:Output 010:NAND_DQ4 011:SDC2_D4 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PC11_SELECT 000:Input 001:Output 010:NAND_DQ3 011:SDC2_D3 100:Reserved 101:Reserved

			110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PC10_SELECT 000:Input 001:Output 010:NAND_DQ2 011:SDC2_D2 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PC9_SELECT 000:Input 001:Output 010:NAND_DQ1 011:SDC2_D1 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PC8_SELECT 000:Input 001:Output 010:NAND_DQ0 011:SDC2_D0 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.12. PC Configure Register 2 (Default Value: 0x0000_0777)

Offset: 0x0050			Register Name: PC_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:8	R/W	0x7	/
7	/	/	/
6:4	R/W	0x7	/
3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000:Input 001:Output 010:NAND_DQS 011:SDC2_RST 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.13. PC Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PC_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	/	/	/

4.21.3.14. PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.15. PC Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x005C			Register Name: PC_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.16. PC Multi-Driving Register 1 (Default Value: 0x0000_0015)

Offset: 0x0060			Register Name: PC_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
[2i+1:2i] (i=0~2)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~18) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.17. PC PULL Register 0 (Default Value: 0x0000_5140)

Offset: 0x0064			Register Name: PC_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x5140	PC_PULL PC[n] Pull-up/down Select (n = 0~15)

			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.18. PC PULL Register 1 (Default Value: 0x0000_0014)

Offset: 0x0068			Register Name: PC_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	Reserved
[2i+1:2i] (i=0~2)	R/W	0x14	PC_PULL PC[n] Pull-up/down Select (n = 16~18) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.19. PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000:Input 001:Output 010:RGMII_TXD3/MII_TXD3/RMII_NULL 011:Reserved 100:TS2_D3 101:TS3_CLK 110:Reserved 111:IO Disable
27	/	/	Reserved
26:24	R/W	0x7	PD6_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_RXERR/RMII_RXER 011:Reserved 100:TS2_D2 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000:Input 001:Output 010:RGMII_RXCTL/MII_RXDV/RMII_CRS_DV 011:Reserved 100:TS2_D1 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD4_SELECT 000:Input 001:Output

			010:RGMII_RXCK/MII_RXCK/RMII_NULL 011:Reserved 100:TS2_D0 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD3_SELECT 000:Input 001:Output 010:RGMII_RXD0/MII_RXD0/RMII_RXD0 011:Reserved 100:TS2_DVLD 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD2_SELECT 000:Input 001:Output 010:RGMII_RXD1/MII_RXD1/RMII_RXD1 011:Reserved 100:TS2_SYNC 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD1_SELECT 000:Input 001:Output 010:RGMII_RXD2/MII_RXD2/RMII_NULL 011:DI_RX 100:TS2_ERR 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD0_SELECT 000:Input 001:Output 010:RGMII_RXD3/MII_RXD3/RMII_NULL 011:DI_TX 100:TS2_CLK 101:Reserved 110:Reserved 111:IO Disable

4.21.3.20. PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD15_SELECT 000:Input 001:Output 010:RGMII_CLKIN/MII_COL/RMII_NULL 011:Reserved 100:SIM1_RST 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/

26:24	R/W	0x7	PD14_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_TXERR/RMII_NULL 011:Reserved 100:SIM1_DATA 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PD13_SELECT 000:Input 001:Output 010:RGMII_TXCTL/MII_TXEN/RMII_TXEN 011:Reserved 100:SIM1_CLK 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PD12_SELECT 000:Input 001:Output 010:RGMII_TXCK/MII_TXCK/RMII_TXCK 011:Reserved 100:SIM1_PWREN 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PD11_SELECT 000:Input 001:Output 010:RGMII_NULL/MII_CRS/RMII_NULL 011:Reserved 100:TS2_D7 101:TS3_D0 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PD10_SELECT 000:Input 001:Output 010:RGMII_TXD0/MII_TXD0/RMII_TXD0 011:Reserved 100:TS2_D6 101:TS3_DVLD 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PD9_SELECT 000:Input 001:Output 010:RGMII_TXD1/MII_TXD1/RMII_TXD1 011:Reserved 100:TS2_D5 101:TS3_SYNC 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD8_SELECT 000:Input 001:Output 010:RGMII_TXD2/MII_TXD2/RMII_NULL 011:Reserved

			100:TS2_D4 110:Reserved	101:TS3_ERR 111:IO Disable

4.21.3.21. PD Configure Register 2 (Default Value: 0x0000_0077)

Offset: 0x0074			Register Name: PD_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x7	PD17_SELECT 000:Input 001:Output 010:MDIO 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PD16_SELECT 000:Input 001:Output 010:MDC 011:Reserved 100:SIM1_DET 101:Reserved 110:Reserved 111:IO Disable

4.21.3.22. PD Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: PD_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.23. PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.24. PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.25. PD Multi-Driving Register 1 (Default Value: 0x0000_0005)

Offset: 0x0084			Register Name: PD_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.26. PD PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.27. PD PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	Reserved
[2i+1:2i] (i=0~1)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.28. PE Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: PE_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PE7_SELECT 000:Input 001:Output 010:CSI_D3 011:TS0_D3 100:TS1_CLK 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE6_SELECT 000:Input 001:Output 010:CSI_D2 011:TS0_D2 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE5_SELECT 000:Input 001:Output 010:CSI_D1 011:TS0_D1 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PE4_SELECT 000:Input 001:Output 010:CSI_D0 011:TS0_D0 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE3_SELECT 000:Input 001:Output 010:CSI_VSYNC 011:TS0_DVLD 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PE2_SELECT 000:Input 001:Output 010:CSI_HSYNC 011:TS0_SYNC 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

7	/	/	/
6:4	R/W	0x7	PE1_SELECT 000:Input 001:Output 010:CSI_MCLK 011:TS0_ERR 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE0_SELECT 000:Input 001:Output 010:CSI_PCLK 011:TS0_CLK 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

4.21.3.29. PE Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0094			Register Name: PE_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PE15_SELECT 000:Input 001:Output 010:Reserved 011:SIM1_VPPPP 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PE14_SELECT 000:Input 001:Output 010:Reserved 011:SIM1_VPPEN 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PE13_SELECT 000:Input 001:Output 010:CSI_SDA 011:TWI2_SDA 100:Reserved 101:Reserved 110:Reserved 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PE12_SELECT 000:Input 001:Output 010:CSI_SCK 011:TWI2_SCK

			100:Reserved 101:Reserved 110:Reserved 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PE11_SELECT 000:Input 001:Output 010:CSI_D7 011:TS0_D7 100:TS1_D0 101:Reserved 110:Reserved 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PE10_SELECT 000:Input 001:Output 010:CSI_D6 011:TS0_D6 100:TS1_DVLD 101:Reserved 110:Reserved 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PE9_SELECT 000:Input 001:Output 010:CSI_D5 011:TS0_D5 100:TS1_SYNC 101:Reserved 110:Reserved 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE8_SELECT 000:Input 001:Output 010:CSI_D4 011:TS0_D4 100:TS1_ERR 101:Reserved 110:Reserved 111:IO Disable

4.21.3.30. PE Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0098			**Register Name: PE_CFG2_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.31. PE Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x009C			**Register Name: PE_CFG3_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.32. PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PE_DATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.33. PE Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x00A4			Register Name: PE_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PE_DRV PE[n] Multi-Driving SELECT (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.34. PE Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: PE_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.35. PE PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: PE_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.36. PE PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PE_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	/	/	/

4.21.3.37. PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PF6_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:PF_EINT6 111:IO Disable
23			
22:20	R/W	0x7	PF5_SELECT 000:Input 001:Output 010:SDC0_D2 011:JTAG_CK 100:Reserved 101:Reserved 110:PF_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PF4_SELECT 000:Input 001:Output 010:SDC0_D3 011:UART0_RX 100:Reserved 101:Reserved 110:PF_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PF3_SELECT 000:Input 001:Output 010:SDC0_CMD 011:JTAG_DO 100:Reserved 101:Reserved 110:PF_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PF2_SELECT 000:Input 001:Output 010:SDC0_CLK 011:UART0_TX 100:Reserved 101:Reserved 110:PF_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PF1_SELECT 000:Input 001:Output

			010:SDC0_D0 011:JTAG_DI 100:Reserved 101:Reserved 110:PF_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PF0_SELECT 000:Input 001:Output 010:SDC0_D1 011:JTAG_MS 100:Reserved 101:Reserved 110:PF_EINT0 111:IO Disable

4.21.3.38. PF Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PF_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.39. PF Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: PF_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.40. PF Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: PF_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.41. PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.42. PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[2i+1:2i] (i=0~6)	R/W	0x1	PF_DRV PF[n] Multi-Driving SELECT (n = 0~6) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.43. PF Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PF_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.44. PF PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[2i+1:2i] (i=0~6)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~6) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.45. PF PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: PF_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.46. PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT

			000:Input 001:Output 010:UART1_RX 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000:Input 001:Output 010:UART1_TX 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000:Input 001:Output 010:SDC1_D3 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000:Input 001:Output 010:SDC1_D2 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG3_SELECT 000:Input 001:Output 010:SDC1_D1 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG2_SELECT 000:Input 001:Output 010:SDC1_D0 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG1_SELECT 000:Input 001:Output 010:SDC1_CMD 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT1 111:IO Disable

3	/	/	/
2:0	R/W	0x7	PG0_SELECT 000:Input 001:Output 010:SDC1_CLK 011:Reserved 100:Reserved 101:Reserved 110:PG_EINT0 111:IO Disable

4.21.3.47. PG Configure Register 1 (Default Value: 0x0077_7777)

Offset: 0x00DC			Register Name: PG_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x7	PG13_SELECT 000:Input 001:Output 010: PCM1_DIN 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT13 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG12_SELECT 000:Input 001:Output 010: PCM1_DOUT 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT12 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG11_SELECT 000:Input 001:Output 010: PCM1_CLK 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG10_SELECT 000:Input 001:Output 010: PCM1_SYNC 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT10 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG9_SELECT 000:Input 001:Output 010:UART1_CTS 011: Reserved

			100:Reserved 101:Reserved 110:PG_EINT9 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PG8_SELECT 000:Input 001:Output 010:UART1_RTS 011: Reserved 100:Reserved 101:Reserved 110:PG_EINT8 111:IO Disable

4.21.3.48. PG Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PG_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.49. PG Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PG_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.50. PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.21.3.51. PG Multi-Driving Register 0 (Default Value: 0x0555_5555)

Offset: 0x00EC			Register Name: PG_DRV0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x1	PG_DRV PG[n] Multi-Driving SELECT (n = 0~13)

			00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.21.3.52. PG Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: PG_DRV1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.53. PG PULL Register 0 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.21.3.54. PG PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PG_PULL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.55. PA External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PA_EINT_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.56. PA External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PA_EINT_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 8~15) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.57. PA External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PA_EINT_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[4i+3:4i] (i=0~5)	R/W	0x0	EINT_CFG External INTn Mode (n = 16~21) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.58. PA External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PA_EINT_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.59. PA External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x210			Register Name: PA_EINT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
[n] (n=0~21)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~21)

			0: Disable 1: Enable

4.21.3.60. PA External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PA_EINT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
[n] (n=0~21)	R/W1C	0x0	EINT_STATUS External INTn Pending Bit (n = 0~21) 0: No IRQ pending 1: IRQ pending Write '1' to clear it.

4.21.3.61. PA External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PA_EINT_DEB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

4.21.3.62. PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PF_EINT_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
[4i+3:4i] (i=0~6)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~6) 0000: Positive Edge 0001: Negative Edge

			0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.63. PF External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PF_EINT_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.64. PF External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PF_EINT_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.65. PF External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PF_EINT_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.66. PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PF_EINT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
[n] (n=0~6)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~6) 0: Disable 1: Enable

4.21.3.67. PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PF_EINT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
[n] (n=0~6)	R/W1C	0x0	EINT_STATUS External INTn Pending Bit (n = 0~6)

			0: No IRQ pending 1: IRQ pending Write '1' to clear it

4.21.3.68. PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PF_EINT_DEB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

4.21.3.69. PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PG_EINT_CFG0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.70. PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PG_EINT_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[4i+3:4i] (i=0~5)	R/W	0x0	EINT_CFG External INTn Mode (n = 8~13)

			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.21.3.71. PG External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PG_EINT_CFG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.72. PG External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: PG_EINT_CFG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.21.3.73. PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PG_EINT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[n] (n=0~13)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~13) 0: Disable 1: Enable

4.21.3.74. PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PG_EINT_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
[n] (n=0~13)	R/W1C	0x0	EINT_STATUS External INTn Pending Bit (n = 0~13) 0: No IRQ pending 1: IRQ pending

			Write ‘1’ to clear it

4.21.3.75. PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PG_EINT_DEB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

4.22. Port Controller (CPUs-PORT)

4.22.1. Overview

The chip has 1 port for multi-functional input/out pins. They are shown below:

- Port L(PL):12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions not used. The external PIO interrupt sources are supported and interrupt mode can be configured by software.

4.22.2. Register List

Module Name	Base Address
PIO	0x01F02C00

Register Name	Offset	Description
PL_CFG0	0x0000	Port L Configure Register 0
PL_CFG1	0x0004	Port L Configure Register 1
PL_CFG2	0x0008	Port L Configure Register 2
PL_CFG3	0x000C	Port L Configure Register 3
PL_DAT	0x0010	Port L Data Register
PL_DRV0	0x0014	Port L Multi-Driving Register 0
PL_DRV1	0x0018	Port L Multi-Driving Register 1
PL_PUL0	0x001C	Port L Pull Register 0
PL_PUL1	0x0020	Port L Pull Register 1
PL_INT_CFG0	0x0200 + 0x00	PIO Interrrupt Configure Register 0
PL_INT_CFG1	0x0200 + 0x04	PIO Interrrupt Configure Register 1
PL_INT_CFG2	0x0200 + 0x08	PIO Interrrupt Configure Register 2
PL_INT_CFG3	0x0200 + 0x0C	PIO Interrrupt Configure Register 3
PL_INT_CTL	0x0200 + 0x10	PIO Interrupt Control Register
PL_INT_STA	0x0200 + 0x14	PIO Interrupt Status Register
PL_INT_DEB	0x0200 + 0x18	PIO Interrupt Debounce Register

4.22.3. Register Description

4.22.3.1. PL Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000	Register Name: PL_CFG0_REG

Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PL7_SELECT 000:Input 001:Output 010:S_JTAG_DI 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PL6_SELECT 000:Input 001:Output 010:S_JTAG_DO 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PL5_SELECT 000:Input 001:Output 010:S_JTAG_CK 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PL4_SELECT 000:Input 001:Output 010:S_JTAG_MS 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PL3_SELECT 000:Input 001:Output 010:S_UART_RX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PL2_SELECT 000:Input 001:Output 010:S_UART_TX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PL1_SELECT

			000:Input 001:Output 010:S_TWI_SDA 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PL0_SELECT 000:Input 001:Output 010:S_TWI_SCK 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT0 111:IO Disable

4.22.3.2. PL Configure Register 1 (Default Value: 0x0000_7777)

Offset: 0x0004			Register Name: PL_CFG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x7	PL11_SELECT 000:Input 001:Output 010:S_CIR_RX 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT11 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PL10_SELECT 000:Input 001:Output 010:S_PWM 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT10 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PL9_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT9 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PL8_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:Reserved 110:S_PL_EINT8 111:IO Disable

4.22.3.3. PL Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PL_CFG2_REG
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

4.22.3.4. PL Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PL_CFG3_REG
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

4.22.3.5. PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

4.22.3.6. PL Multi-Driving Register 0 (Default Value: 0x0055_5555)

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PL_DRV PL[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

4.22.3.7. PL Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

4.22.3.8. PL PULL Register 0 (Default Value: 0x0000_0005)

Offset: 0x001C			Register Name: PL_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x5	PL_PULL PL[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

4.22.3.9. PL PULL Register 1 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PL_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.22.3.10. PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PL_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	EINT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.22.3.11. PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
[4i+3:4i] (i=0~3)	R/W	0x0	EINT_CFG External INTn Mode (n = 8~11) 0000: Positive Edge 0001: Negative Edge 0010: High Level

			0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

4.22.3.12. PL External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PL_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.22.3.13. PL External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PL_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

4.22.3.14. PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[n] (n=0~11)	R/W	0x0	EINT_CTL External INTn Enable (n = 0~11) 0: Disable 1: Enable

4.22.3.15. PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[n] (n=0~11)	R/W	0x0	EINT_STATUS External INTn Pending Bit (n = 0~11) 0: No IRQ pending 1: IRQ pending Write '1' to clear

4.22.3.16. PL External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

Chapter 5 Memory

This section describes the H5 memory from three aspects:

- DRAMC
- NDFC
- SMHC

5.1. SDRAM Controller(DRAMC)

5.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to the industy-standard DDR3/DDR3L SDRAM. It supports up to a 24G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

Features:

- 32-bit bus width
- Supports 2 chip selects
- Supports DDR3/DDR3L SDRAM
- Supports power voltage of 1.5V and 1.35V
- Supports clock frequency up to 667 MHz(DDR3-1333)
- Supports memory capacity up to 24G bits (3G bytes)
- Supports 16 address lines and 3 bank address lines
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Priority of transferring through multiple ports is programmable
- Random read or write operation is supported

5.2. NAND Flash Controller(NDFC)

5.2.1. Overview

The NAND Flash Controller(NDFC) supports all NAND flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three modes are supported for serial read access. Mode 0 is for the conventional serial access and mode 1 is for EDO type and mode 2 for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

Features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Supports 8-bit data bus width
- Supports 1024, 2048, 4096, 8192, 16384 bytes size per page
- Supports conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
- Corrected error bits number information report
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers
- One Command FIFO
- Embedded DMA to do data transfer
- External DMA is supported for transferring data
- Two 256x32-bit RAM for Pipeline Procession
- Support SDR, ONFI DDR and Toggle DDR NAND
- Support self–debug for NDFC debug

5.2.2. Block Diagram

The NDFC system block diagram is shown below:

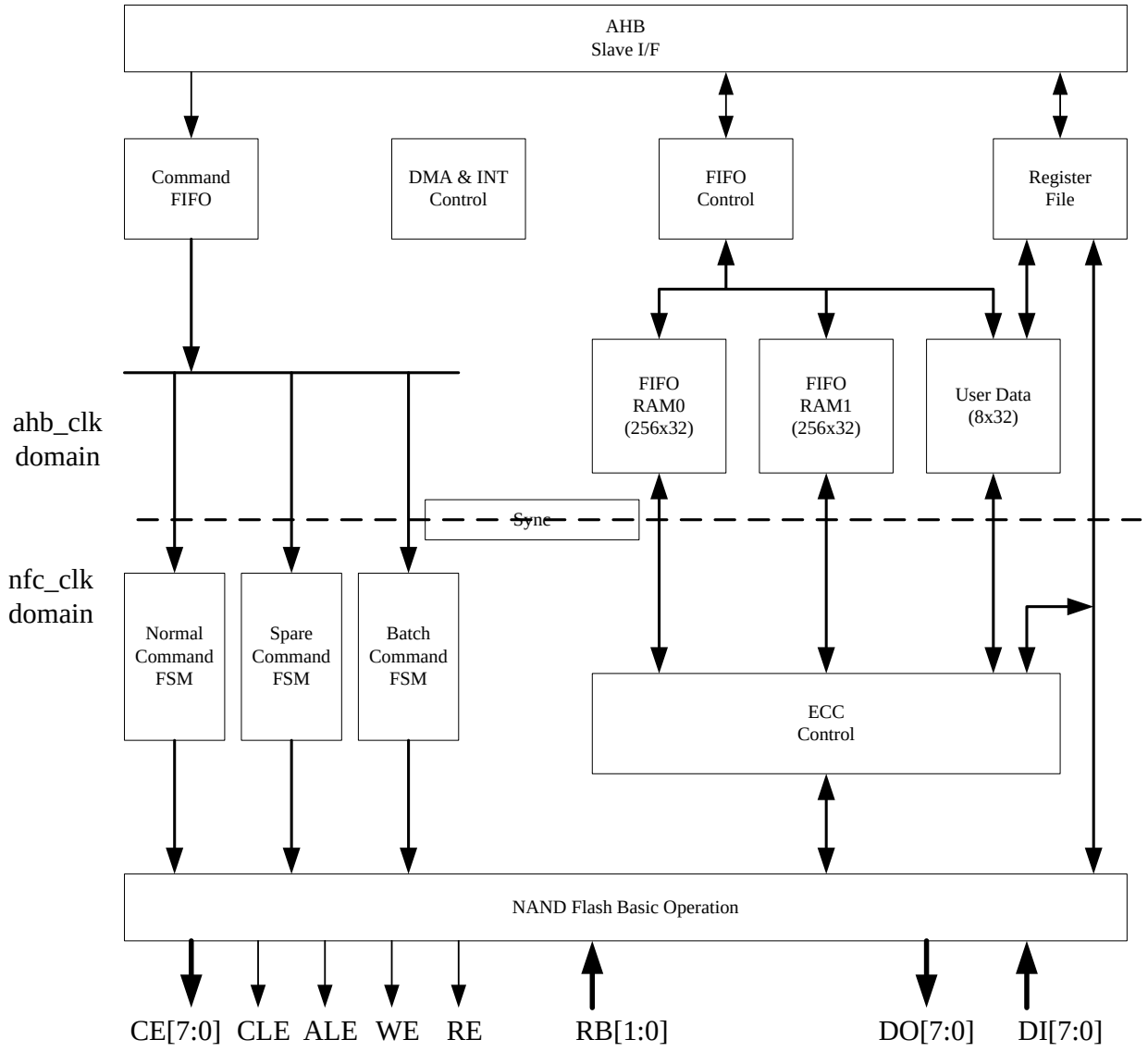


Figure 5-1. NDFC Block Diagram

5.2.3. Operations and Functional Descriptions

5.2.3.1. External Signals

Table 5-1 describes the external signals of NDFC.DQ0~DQ7 and DQS are bidirectional I/O.WE,ALE,CLE,CE,RE are output pin, RB is input pin. The RB pin in the NAND device is an open-drain driver, which must need a pull-up resistor.

Table 5-1. NDFC External Signals

Signals	Description	Type
NAND_WE	Write Enable	O
NAND_ALE	Address Latch Enable,High Active	O

NAND_CLE	Command Latch Enable,High Active	O
NAND_CE0	Chip Enable 0,Low Active	O
NAND_CE1	Chip Enable 1,Low Active	O
NAND_RE	Read Enable	O
NAND_RB0	Read/Busy 0,Low Active	I
NAND_RB1	Read/Busy 1,Low Active	I
NAND_DQ0	Data Input and Output	I/O
NAND_DQ1	Data Input and Output	I/O
NAND_DQ2	Data Input and Output	I/O
NAND_DQ3	Data Input and Output	I/O
NAND_DQ4	Data Input and Output	I/O
NAND_DQ5	Data Input and Output	I/O
NAND_DQ6	Data Input and Output	I/O
NAND_DQ7	Data Input and Output	I/O
NAND_DQS	Data Strobe	I/O

5.2.3.2. Clock Sources

NDFC gets three different clocks. Users can select one of them to make NDFC clock source. Table 5-2 describles the clock sources of NDFC. Users can see **CCU** for clock setting, configuration and gating information.

Table 5-2. NDFC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock,the default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock,the default value is 600MHz

5.2.3.3. NDFC Timing Diagram

Typically, there are two kinds of serial access methods. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.

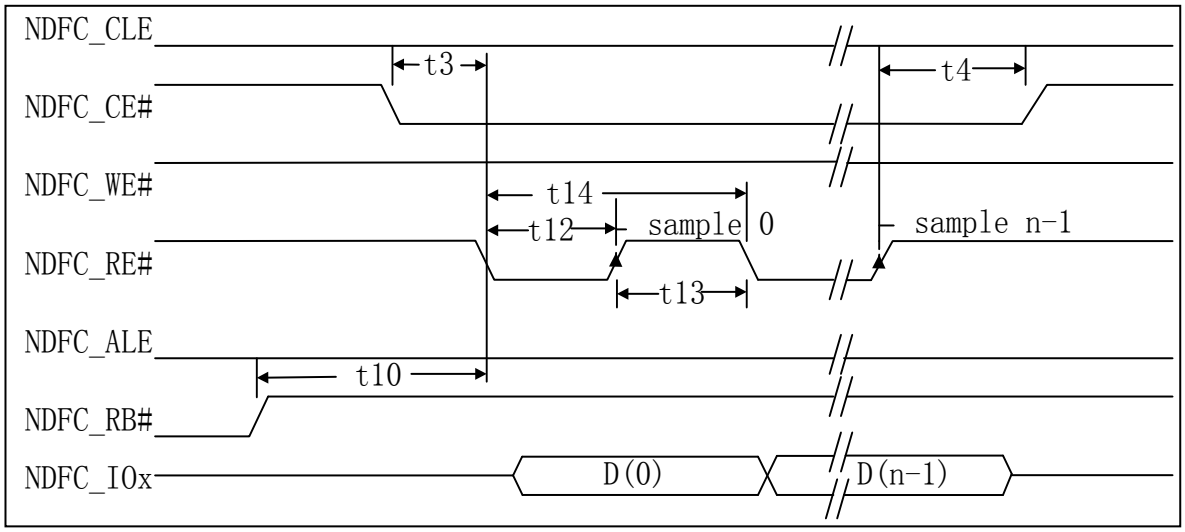


Figure 5-2. Conventional Serial Access Cycle Diagram (SAM0)

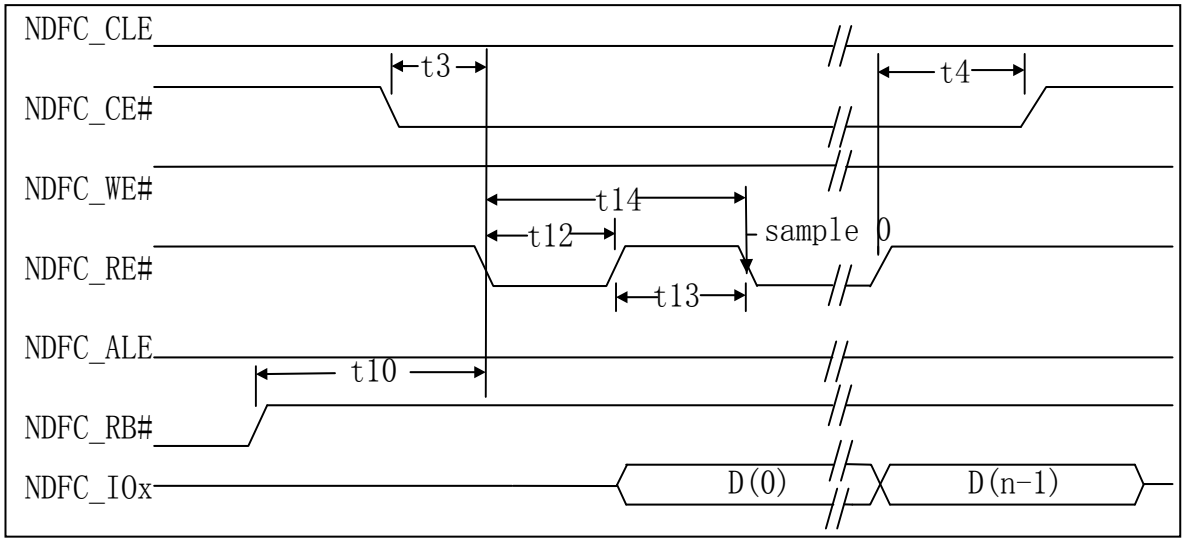


Figure 5-3. EDO Type Serial Access after Read Cycle (SAM1)

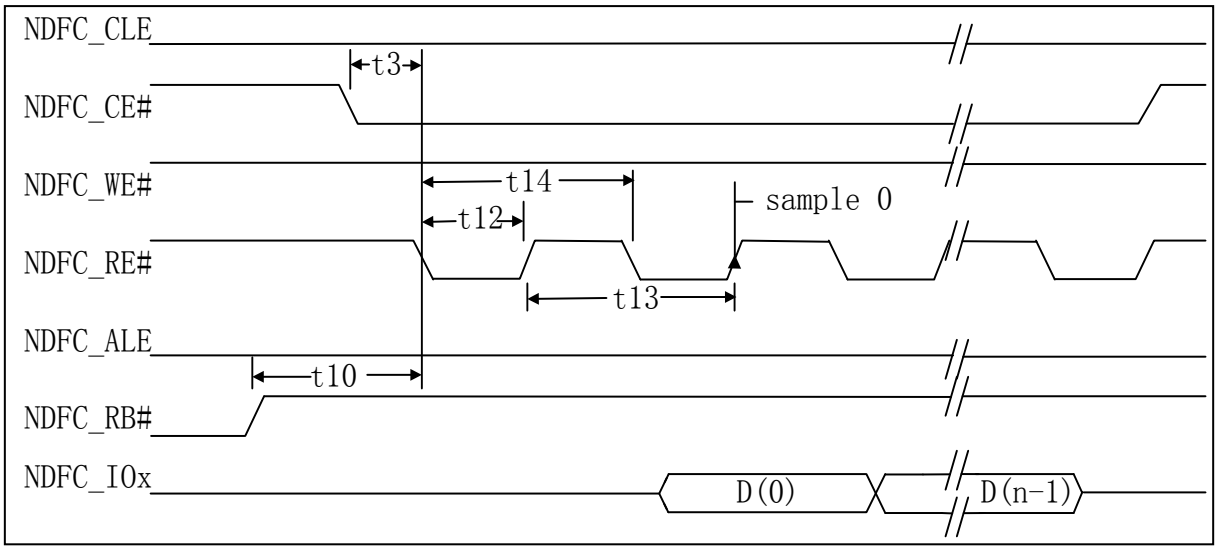


Figure 5-4. Extending EDO Type Serial Access Mode (SAM2)

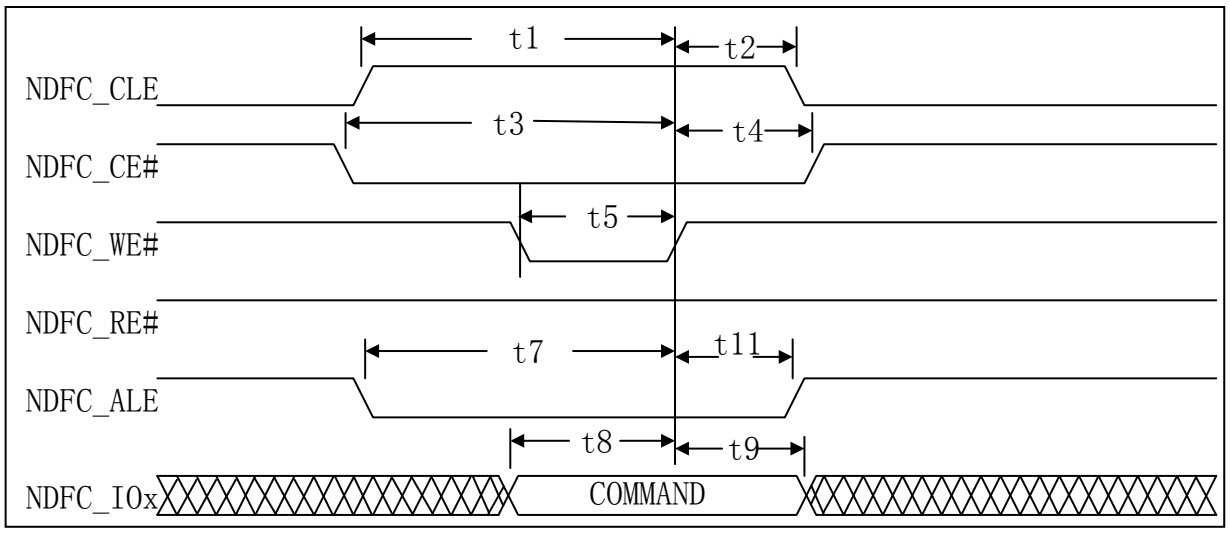


Figure 5-5. Command Latch Cycle

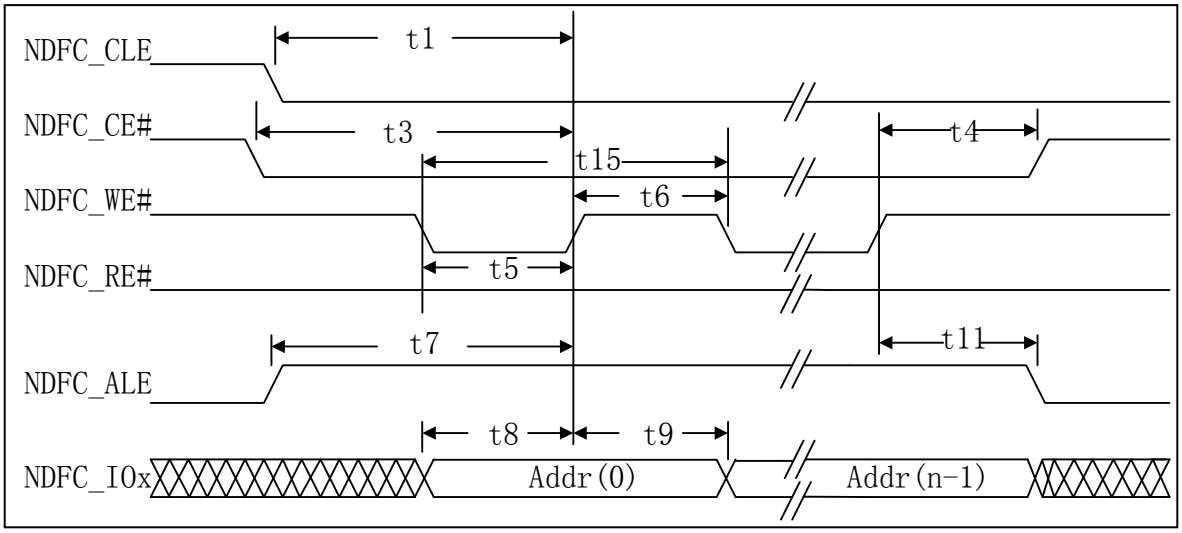


Figure 5-6. Address Latch Cycle

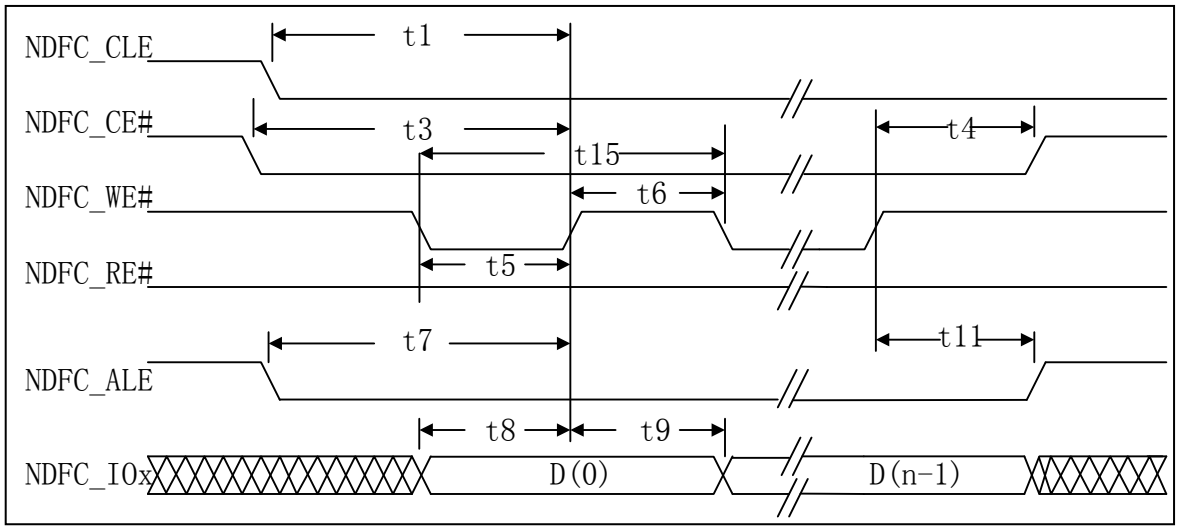


Figure 5-7. Write Data to Flash Cycle

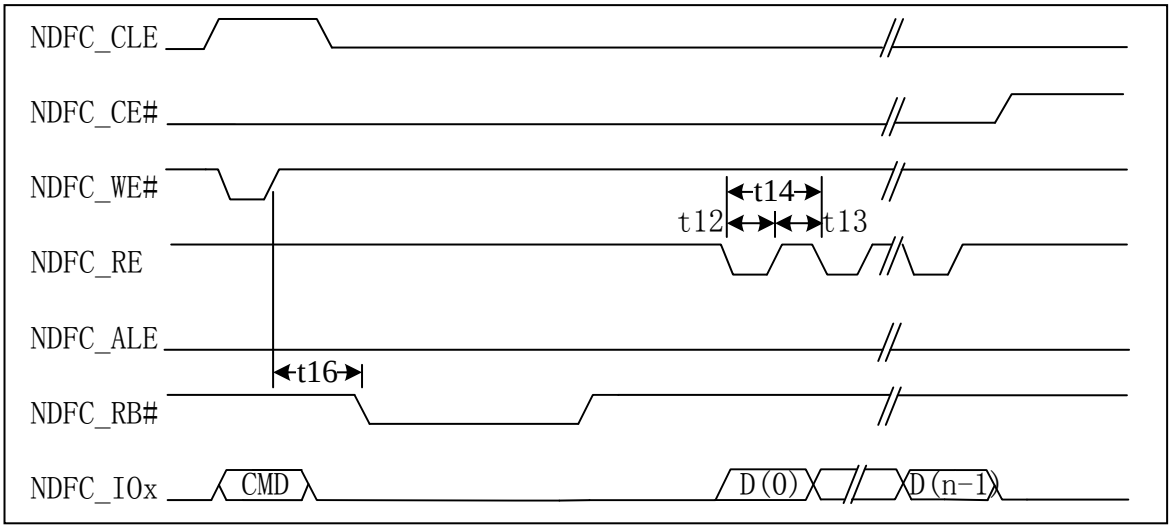


Figure 5-8. Waiting R/B# Ready Diagram

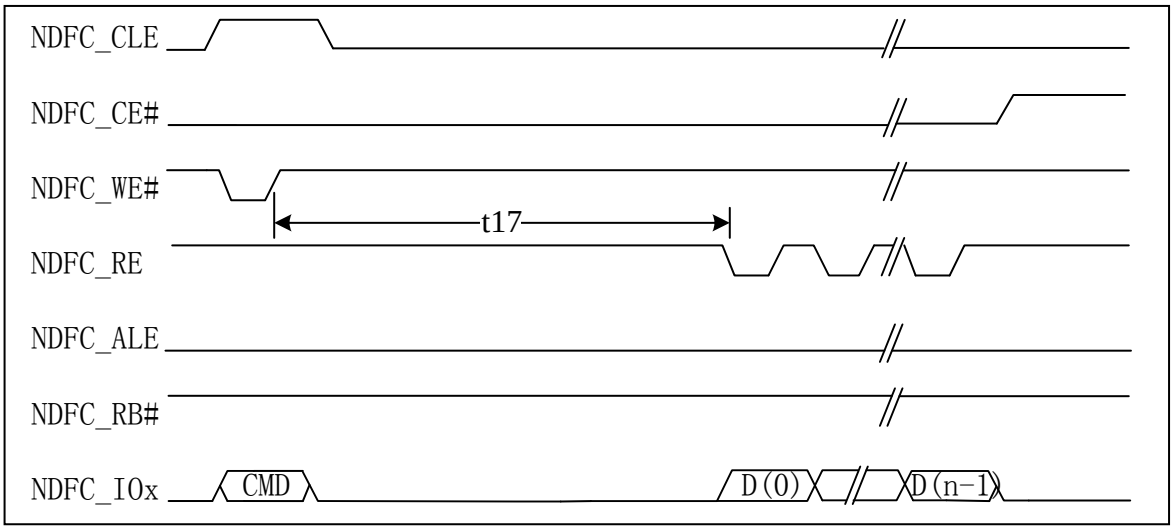


Figure 5-9. WE# High to RE# Low Timing Diagram

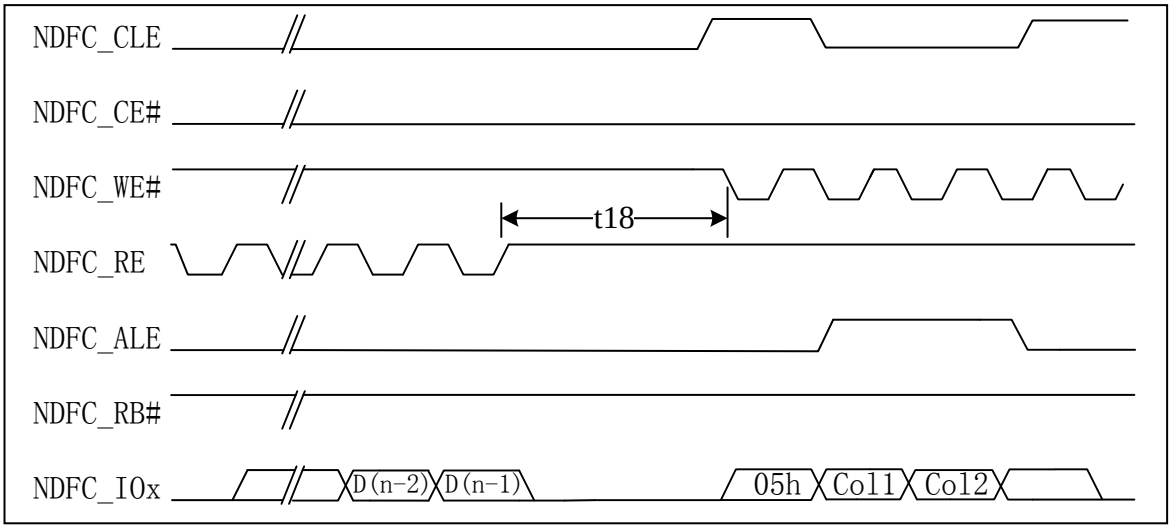


Figure 5-10. RE# High to WE# Low Timing Diagram

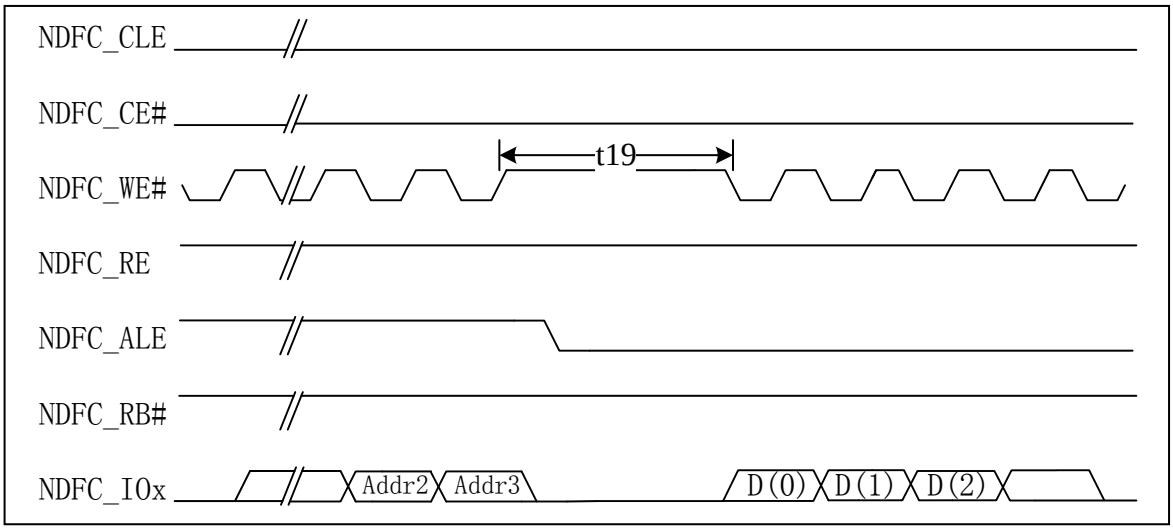


Figure 5-11. Address to Data Loading Timing Diagram

Timing cycle list:

ID	Parameter	Timing	Notes
t1	NDFC_CLE setup time	2T	
t2	NDFC_CLE hold time	2T	
t3	NDFC_CE setup time	2T	
t4	NDFC_CE hold time	2T	
t5	NDFC_WE# pulse width	T(1)	
t6	NDFC_WE# hold time	T	
t7	NDFC_ALE setup time	2T	
t8	Data setup time	T	
t9	Data hold time	T	

t10	Ready to NDFC_RE# low	3T	
t11	NDFC_ALE hold time	2T	
t12	NDFC_RE# pulse width	T	
t13	NDFC_RE# hold time	T	
t14	Read cycle time	2T	
t15	Write cycle time	2T	
t16	NDFC_WE# high to R/B# busy	T_WB(2)	Specified by timing configure register (NDFC_TIMING_CFG)
t17	NDFC_WE# high to NDFC_RE# low	T_WHR(3)	Specified by timing configure register (NDFC_TIMING_CFG)
t18	NDFC_RE# high to NDFC_WE# low	T_RHW(4)	Specified by timing configure register (NDFC_TIMING_CFG)
t19	Address to Data Loading time	T_ADL(5)	Specified by timing configure register (NDFC_TIMING_CFG)
Note(1): T is the cycle of the internal clock. **Note(2),(3),(4),(5)**: These values are configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 8*2T/16*2T/24*2T/32*2T, the value of T_RHW could be 4*2T/8*2T/12*2T/20*2T, the value of T_ADL could be 0*2T/8*2T/16*2T/24*2T.			

5.2.3.4. NDFC Operation Guide

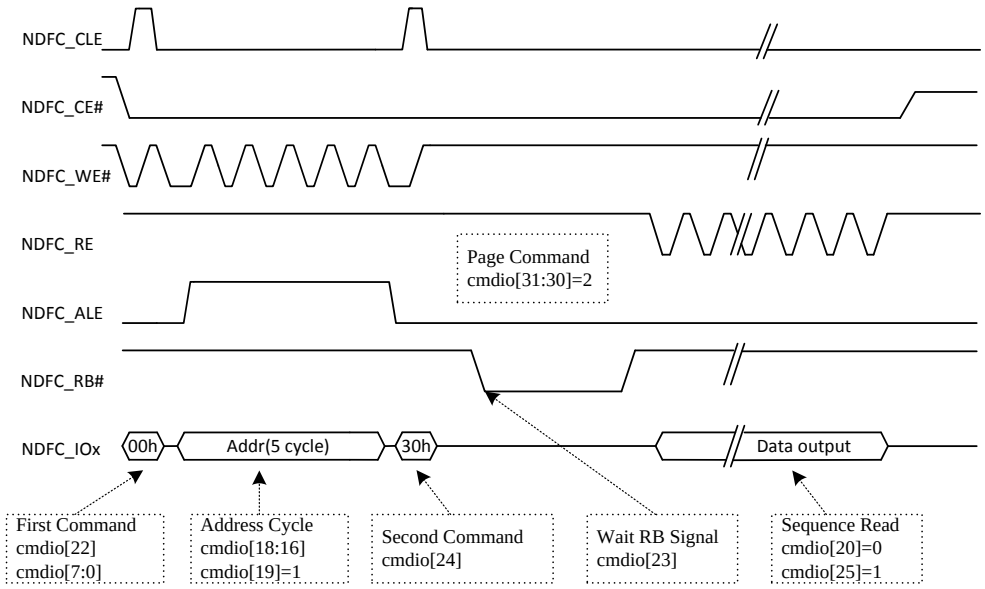


Figure 5-12. Page Read Command Diagram

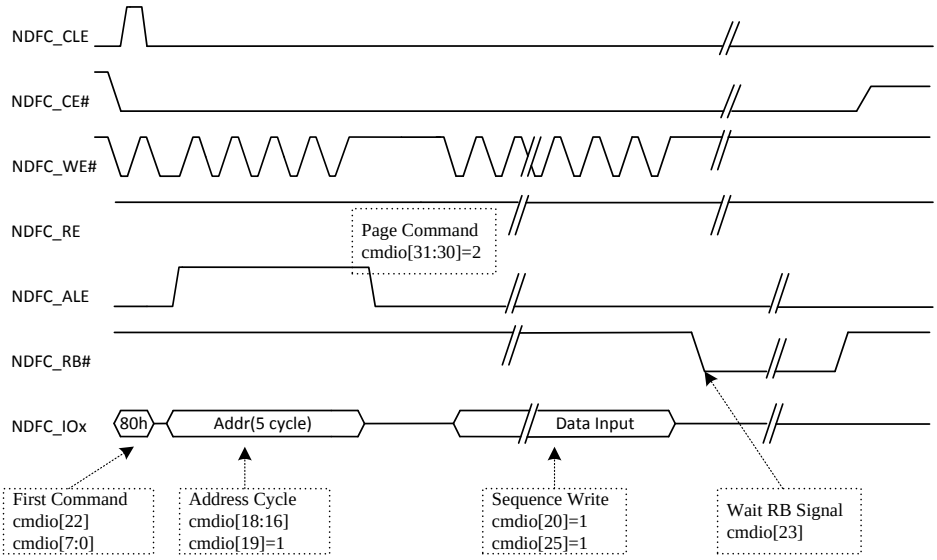


Figure 5-13. Page Program Diagram

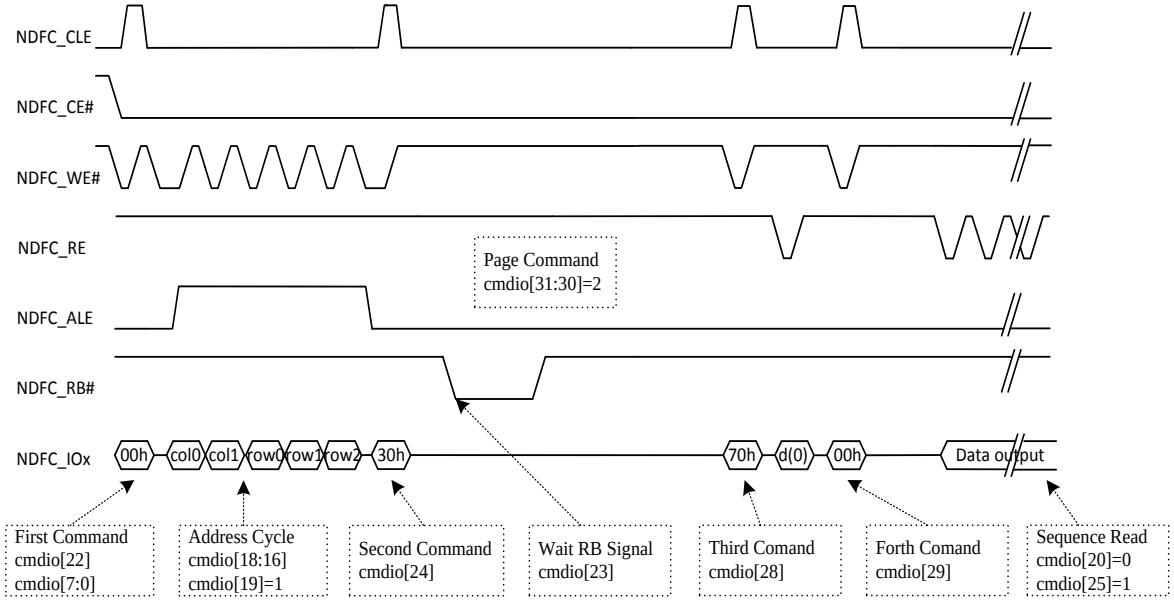


Figure 5-14. EF-NAND Page Read Diagram

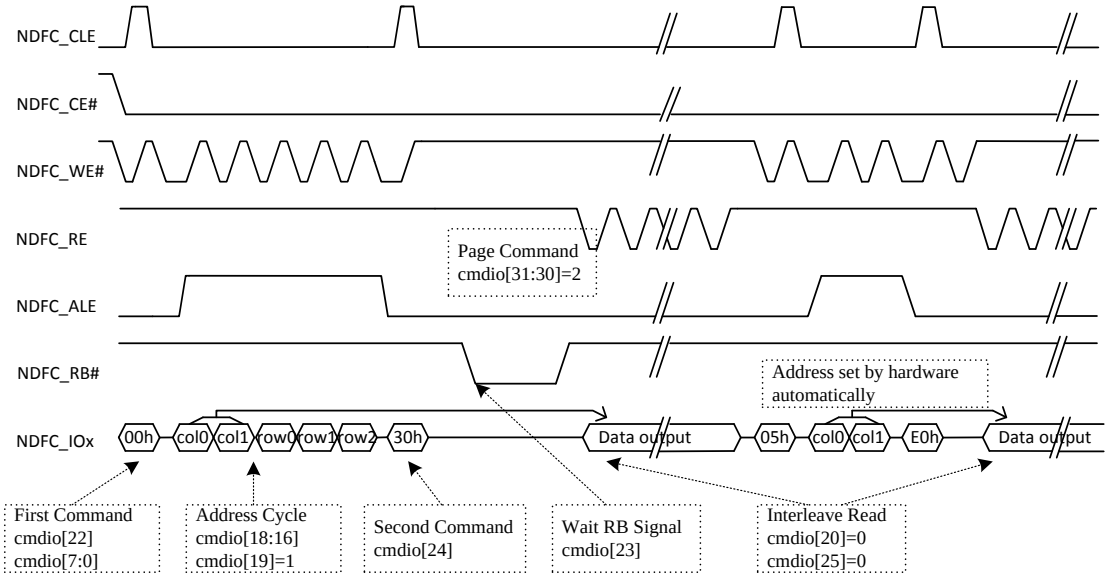


Figure 5-15. Interleave Page Read Diagram

5.2.4. Register List

Module Name	Base Address
NDFC	0x01C03000

Register Name	Offset	Description
NDFC_CTL	0x0000	NDFC Configure and Control Register
NDFC_ST	0x0004	NDFC Status Information Register
NDFC_INT	0x0008	NDFC Interrupt Control Register
NDFC_TIMING_CTL	0x000C	NDFC Timing Control Register
NDFC_TIMING_CFG	0x0010	NDFC Timing Configure Register
NDFC_ADDR_LOW	0x0014	NDFC Low Word Address Register
NDFC_ADDR_HIGH	0x0018	NDFC High Word Address Register
NDFC_BLOCK_NUM	0x001C	NDFC Data Block Number Register
NDFC_CNT	0x0020	NDFC Data Counter for Data Transfer Register
NDFC_CMD	0x0024	Set up NDFC commands Register
NDFC_RCMD_SET	0x0028	Read Command Set Register for Vendor's NAND Memory
NDFC_WCMD_SET	0x002C	Write Command Set Register for Vendor's NAND Memory
NDFC_ECC_CTL	0x0034	ECC Configure and Control Register
NDFC_ECC_ST	0x0038	ECC Status and Operation information Register
NDFC_EFR	0x003C	Enhanced Feature Register
NDFC_ERR_CNT0	0x0040	Corrected Error Bit Counter Register 0
NDFC_ERR_CNT1	0x0044	Corrected Error Bit Counter Register 1
NDFC_USER_DATAn	0x0050 + N*0x04	User Data Field Register N (N from 0 to 15)
NDFC_EFNAND_STA	0x0090	EFNAND Status Register
NDFC_SPARE_AREA	0x00A0	Spare Area Configure Register

NDFC_PAT_ID	0x00A4	Pattern ID Register
NDFC_RDATA_STA_CTL	0x00A8	Read Data Status Control Register
NDFC_RDATA_STA_0	0x00AC	Read Data Status Register 0
NDFC_RDATA_STA_1	0x00B0	Read Data Status Register 1
NDFC_MDMA_ADDR	0x00C0	MBUS DMA Address Register
NDFC_MDMA_CNT	0x00C4	MBUS DMA Data Counter Register
NDFC_NDMA_MODE_CTL	0x00D0	NDFC Normal DMA Mode Control Register
NDFC_IO_DATA	0x0300	Data Input/Output Port Address Register
RAM0_BASE	0x0400	1024 Bytes RAM0 Base
RAM1_BASE	0x0800	1024 Bytes RAM1 Base

5.2.5. Register Description

5.2.5.1. NDFC Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: NDFC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	NDFC_CE_SEL Chip Select for 8 NAND Flash Chips 0000~0111: NDFC Chip Select Signal 0-7 is selected 1000~1111: NDFC CS[7:0] not selected. GPIO pins can be used for CS. NDFC can support up to 16 CS.
23:22	/	/	/
21	R/W	0x0	NDFC_DDR_RM DDR Repeat data mode 0: Lower byte 1: Higher byte
20	R/W	0x0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0x0	NF_TYPE NAND Flash Type 00: Normal SDR NAND 01: Reserved 10: ONFI DDR NAND 11: Toggle DDR NAND
17	R/W	0x0	NDFC_CLE_POL

			NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0x0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0x0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0x0	NDFC_RAM_METHOD Access internal RAM method 0: Access internal RAM by AHB bus 1: Access internal RAM by DMA bus
13:12	/	/	/
11:8	R/W	0x0	NDFC_PAGE_SIZE 0000: 1024 bytes 0001: 2048 bytes 0010: 4096 bytes 0011: 8192 bytes 0100: 16384 bytes **Note:** The page size is for main field data.
7	/	/	/
6	R/W	0x0	NDFC_CE_ACT Chip select signal CE# control during NAND operation 0: De-active chip select signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatically controls chip select signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled.
5	/	/	/
4:3	R/W	0x0	NDFC_RB_SEL NDFC external R/B signal select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0x0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus

1	R/W	0x0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset
0	R/W	0x0	NDFC_EN NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

5.2.5.2. NDFC Status Register (Default Value: 0x0000_0F00)

Offset: 0x0004			Register Name: NDFC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is greater threshold value. 1: The number of bit 1 during current read operation is less than or equal to threshold value. This field only is valid when **NDFC_RDATA_STA_EN** is 1. The threshold value is configured in **NDFC_RDATA_STA_TH**.
12	R	0x0	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is greater threshold value. 1: The number of bit 0 during current read operation is less than or equal to than threshold value. This field only is valid when **NDFC_RDATA_STA_EN** is 1. The threshold value is configured in **NDFC_RDATA_STA_TH**.
11	R	0x1	NDFC_RB_STATE3 NAND Flash R/B 3 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	0x1	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	0x1	NDFC_RB_STATE1 NAND Flash R/B 1 Line State

			0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	0x1	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0x0	NDFC_STA 0: NDFC FSM in IDLE State 1: NDFC FSM in BUSY State When **NDFC_STA** is 0, NDFC can accept new command and process command.
3	R	0x0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W1C	0x0	NDFC_DMA_INT_FLAG When it is 1, it means that a pending DMA is completed. It will be cleared after writing 1 to this bit or it will be automatically clear before FSM processing an new command.
1	R/W1C	0x0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command Mode or one Batch Command Work Mode. It will be cleared after writing 1 to this bit or it will be automatically clear before FSM processing an new command.
0	R/W1C	0x0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be cleared after writing 1 to this bit.

5.2.5.3. NDFC Interrupt and DMA Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: NDFC_INT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.
1	R/W	0x0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a

			single command in Normal Command Work Mode or one Batch Command Work Mode. 0: Disable 1: Enable
0	R/W	0x0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state. 0: Disable 1: Enable

5.2.5.4. NDFC Timing Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: NDFC_TIMING_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	NDFC_READ_PIPE In SDR mode: 0000: Normal 0001: EDO 0010: E-EDO Other : Reserved In DDR mode: 0001~1111 is valid.(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0x0	NDFC_DC_CTL NDFC Delay Chain Control. These bits are only valid in DDR data interface, and configure the relative phase between DQS and DQ[0…7]

5.2.5.5. NDFC Timing Configure Register (Default Value: 0x0000_0095)

Offset: 0x0010			Register Name: NDFC_TIMING_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	T_WC Write Cycle Time 00: 1*2T

			01: 2*2T 10: 3*2T 11: 4*2T
17:16	R/W	0x0	T_CCS Change Column Setup Time 00: 16*2T 01: 24*2T 10: 32*2T 11: 64*2T
15:14	R/W	0x0	T_CLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0x0	T_CS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0x0	T_CDQSS DQS Setup Time for Data Input Start 0: 8*2T 1: 24*2T
10:8	R/W	0x0	T_CAD Command, Address, Data Delay 000: 4*2T 001: 8*2T 010: 12*2T 011: 16*2T 100: 24*2T 101: 32*2T 110/111: 64*2T
7:6	R/W	0x2	T_RHW RE# High to WE# Low Cycle Number 00: 4*2T 01: 8*2T 10: 12*2T

			11: 20*2T
5:4	R/W	0x1	T_WHR WE# High to RE# Low Cycle Number 00: 8*2T 01: 16*2T 10: 24*2T 11: 32*2T
3:2	R/W	0x1	T_ADL Address to Data Loading Cycle Number 00: 0*2T 01: 8*2T 10: 16*2T 11: 24*2T
1:0	R/W	0x1	T_WB WE# High to Busy Cycle Number 00:14*2T 01:22*2T 10: 30*2T 11:38*2T

5.2.5.6. NDFC Address Low Word Register (Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: NDFC_ADDR_LOW**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA4 NAND Flash 4th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA3 NAND Flash 3rd Cycle Address Data
15:8	R/W	0x0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0x0	ADDR_DATA1 NAND Flash 1st Cycle Address Data

5.2.5.7. NDFC Address High Word Register (Default Value: 0x0000_0000)

Offset: 0x0018			**Register Name: NDFC_ADDR_HIGH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA7

			NAND Flash 7th Cycle Address Data
15:8	R/W	0x0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0x0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

5.2.5.8. NDFC Data Block Number Register (Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: NDFC_DATA_BLOCK_NUM**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	NDFC_DATA_BLOCK_NUM DATA BLOCK Number It is used for batch command procession. 00000: no data 00001: 1 data blocks 000010: 2 data blocks … 10000: 16 data blocks Others: Reserved **Note:** 1 data block = 512 or 1024 bytes main field data

5.2.5.9. NDFC Data Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: NDFC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	NDFC_DATA_CNT Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

5.2.5.10. NDFC Command IO Register (Default Value: 0x0000_0000)

Offset: 0x0024			**Register Name: NDFC_CMD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	NDFC_CMD_TYPE 00: Common Command for normal operation 01: Special Command for Flash Spare Field Operation

			10: Page Command for batch process operation 11: Reserved
29	R/W	0x0	NDFC_SEND_FOURTH_CMD 0: Don't send third set command 1: Send it on the external memory's bus **Note:** It is used for EF-NAND page read.
28	R/W	0x0	NDFC_SEND_THIRD_CMD 0: Don't send third set command 1: Send it on the external memory's bus **Note:** It is used for EF-NAND page read.
27	R/W	0x0	NDFC_ROW_ADDR_AUTO Row address auto increase for page command 0: Normal operation 1: Row address increasing automatically
26	R/W	0x0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for common command and special command. 0: No action 1: DMA transfer automatically It only is active when **NDFC_DATA_METHOD** is 1. If this bit is set to 1, NDFC should setup DRQ to fetch data before output to Flash, or NDFC should setup DRQ to send out to system memory after fetching data from Flash. If this bit is set to 0, NDFC outputs the data to internal RAM or do nothing after fetching data from Flash.
25	R/W	0x0	NDFC_SEQ User data & BCH check word position. It only is active for page command, don't care about this bit for other two commands. 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0x0	NDFC_SEND_SECOND_CMD 0: Don't send the second set command 1: Send it on the external memory's bus
23	R/W	0x0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY;

			otherwise it can't when the internal NDFC_RB wire is BUSY.
22	R/W	0x0	NDFC_SEND_FIRST_CMD 0: Don't send the first set command 1: Send it on the external memory's bus
21	R/W	0x0	NDFC_DATA_TRANS 0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field **NDFC_ACCESS_DIR**.
20	R/W	0x0	NDFC_ACCESS_DIR 0: Read NAND Flash 1: Write NAND Flash
19	R/W	0x0	NDFC_SEND_ADR 0: Don't send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by the field **NDFC_ADR_NUM**.
18:16	R/W	0x0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field 111: 8 cycles address field
15:8	R/W	0x0	NDFC_CMD_HIGH_BYTE NDFC Command High Byte Data If 8-bit command is supported, the high byte should be zero for 16-bit bus width NAND Flash. For 8-bit bus width NAND Flash, high byte command is discarded.
7:0	R/W	0x0	NDFC_CMD_LOW_BYTE NDFC Command Low Byte Data This command will be sent to external Flash by NDFC.

5.2.5.11. NDFC Command Set Register 0 (Default Value: 0x00E0_0530)

Offset: 0x0028			**Register Name: NDFC_CMD_SET0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1

			Used for batch read operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for batch read operation
7:0	R/W	0x30	NDFC_READ_CMD Used for batch read operation

5.2.5.12. NDFC Command Set Register 1 (Default Value: 0x7000_8510)

Offset: 0x002C			**Register Name: NDFC_CMD_SET1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x70	NDFC_READ_CMD0 Used for EF-NAND page read operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND page read operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for batch write operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for batch write operation

5.2.5.13. NDFC ECC Control Register (Default Value: 0x4A80_0008)

Offset: 0x0034			**Register Name: NDFC_ECC_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x4A80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when **NDFC_RANDOM_EN** is set to '1'.
15:12	R/W	0x0	NDFC_ECC_MODE 0000: BCH-16 for one ECC Data Block 0001: BCH-24 for one ECC Data Block 0010 : BCH-28 for one ECC Data Block 0011 : BCH-32 for one ECC Data Block 0100 : BCH-40 for one ECC Data Block 0101 : BCH-48 for one ECC Data Block 0110 : BCH-56 for one ECC Data Block 0111 : BCH-60 for one ECC Data Block 1000 : BCH-64 for one ECC Data Block Others: Reserved
11	R/W	0x0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size

10	R/W	0x0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
9	R/W	0x0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
8:6	/	/	/
5	R/W	0x0	NDFC_ECC_BLOCK_SIZE 0: 1024 bytes of one ECC data block 1: 512 bytes of one ECC data block
4	R/W	0x0	NDFC_ECC_EXCEPTION 0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. **Note:** It only is active when ECC is ON
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error correction function no pipeline with next block operation 1: Error correction pipeline
2:1	/	/	/
0	R/W	0x0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

5.2.5.14. NDFC ECC Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: NDFC_ECC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	NDFC_PAT_FOUND Special Pattern (all 0x00 or all 0xff) Found Flag for 16 Data Blocks 0: No Found 1: Special pattern is found When this field is '1', this means that the special data is found for reading external NAND flash. The **NDFC_PAT_ID** register indicates which pattern is

			found.
15:0	R	0x0	NDFC_ECC_ERR Error information bit of 16 Data Blocks 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them **Note:** The LSB of this register is corresponding the 1st ECC data block. 1 ECC Data Block = 512 or 1024 bytes.

5.2.5.15. NDFC Enhanced Feature Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: NDFC_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	R/W	0x0	/
8	R/W	0x0	NDFC_WP_CTRL NAND Flash Write Protect Control Bit 0: Write Protect is active 1: Write Protect is not active **Note:** When this bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0x0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, the special bits error are inserted before writing external Flash Memory. 0: No error is inserted (ECC Normal Operation) n: N bits error are inserted

5.2.5.16. NDFC Error Counter Register 0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: NDFC_ERR_CNT0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[3] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits …

			01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
23:16	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[3] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
15:8	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[3] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
7:0	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[3] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes

5.2.5.17. NDFC Error Counter Register 1 (Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: NDFC_ERR_CNT1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[7]

			00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
23:16	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[6] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
15:8	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[5] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
7:0	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[4] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes

5.2.5.18. NDFC Error Counter Register 2 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: NDFC_ERR_CNT2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[11] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
23:16	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[10] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
15:8	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[9] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
7:0	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[8] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits

			Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes

5.2.5.19. NDFC Error Counter Register 3 (Default Value: 0x0000_0000)

Offset: 0x004C			**Register Name: NDFC_ERR_CNT3**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[15] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
23:16	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[14] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
15:8	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[13] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes
7:0	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[12]

			00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits … 01000000: 64 corrected bits Others: Reserved **Note:** 1 ECC Data Block = 512 or 1024 bytes

5.2.5.20. NDFC User Data Register [N] (Default Value: 0xFFFF_FFFF)

Offset: 0x0050 + N*0x04 (N=0~15)			Register Name: NDFC_USER_DATAN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xffffffff	USER_DATA User data for ECC Data Block[N] (N from 0 to 15) **Note:** 1 ECC Data Block = 512 or 1024 bytes

5.2.5.21. NDFC EFNAND STATUS Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: NDFC_EFNAND_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	EF_NAND_STATUS The status value for EF-NAND page read operation

5.2.5.22. NDFC Spare Area Register (Default Value: 0x0000_0400)

Offset: 0x00A0			Register Name: NDFC_SPARE_AREA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the first byte address of the spare area for NDFC interleave page operation.

5.2.5.23. NDFC Pattern ID Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: NDFC_PAT_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R	0x0	PAT_ID Special Pattern ID for ECC data block[15]

			0: All 0x00 is found 1: All 0xFF is found Others: Reserved
29:28	R	0x0	PAT_ID Special Pattern ID for ECC data block[14] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
27:26	R	0x0	PAT_ID Special Pattern ID for ECC data block[13] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
25:24	R	0x0	PAT_ID Special Pattern ID for ECC data block[12] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
23:22	R	0x0	PAT_ID Special Pattern ID for ECC data block[11] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
21:20	R	0x0	PAT_ID Special Pattern ID for ECC data block[10] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
19:18	R	0x0	PAT_ID Special Pattern ID for ECC data block[9] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
17:16	R	0x0	PAT_ID Special Pattern ID for ECC data block[8] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved

15:14	R	0x0	PAT_ID Special Pattern ID for ECC data block[7] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
13:12	R	0x0	PAT_ID Special Pattern ID for ECC data block[6] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
11:10	R	0x0	PAT_ID Special Pattern ID for ECC data block[5] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
9:8	R	0x0	PAT_ID Special Pattern ID for ECC data block[4] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
7:6	R	0x0	PAT_ID Special Pattern ID for ECC data block[3] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
5:4	R	0x0	PAT_ID Special Pattern ID for ECC data block[2] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
3:2	R	0x0	PAT_ID Special Pattern ID for ECC data block[1] 0: All 0x00 is found 1: All 0xFF is found Others: Reserved
1:0	R	0x0	PAT_ID Special Pattern ID for ECC data block[0]

			0: All 0x00 is found 1: All 0xFF is found Others: Reserved

5.2.5.24. NDFC Read Data Status Control Register (Default Value: 0x0100_0000)

Offset: 0x00A8			Register Name: NDFC_RDATA_STA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN 0: Disable to count the number of bit 1 and bit 0 during current read operation. 1: Enable to count the number of bit 1 and bit 0 during current read operation. The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:18	/	/	/
17:0	R/W	0x0	NDFC_RDATA_STA_TH The threshold value to generate data status. If the number of bit 1 during current read operation is less than or equal to threshold value, the **NDFC_RDATA_STA_0** bit will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, the **NDFC_RDATA_STA_1** bit will be set.

5.2.5.25. NDFC Read Data Status Register 0 (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: NDFC_RDATA_STA_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when next command is executed.

5.2.5.26. NDFC Read Data Status Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: NDFC_RDATA_STA_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when next command is executed.

5.2.5.27. NDFC MBUS DMA Address Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: NDFC_MDMA_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MDMA_ADDR MBUS DMA address

5.2.5.28. NDFC MBUS DMA Byte Counter Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: NDFC_MDMA_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	0x0	MDMA_CNT MBUS DMA data counter

5.2.5.29. NDFC Normal DMA Mode Control Register (Default Value: 0x0000_00A5)

Offset: 0x00D0			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA5	NDMA_MODE_CTL 0xEA: NDMA handshake mode Note: NDMA wait mode don't care this value.0xA5 can be also used in handshake mode, but 0xEA is better.

5.2.5.30. NDFC IO Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: NDFC_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_IO_DATA Read/Write data into the internal RAM Access unit is 32-bit.

5.3. SD/MMC Host Controller(SMHC)

5.3.1. Overview

The SD/MMC Host Controller(SMHC) provides three controllers including SD card,MMC and SDIO device. SMHC controls the read/write operations on the secure digital(SD) card ,multimedia card(MMC), and supports extended Wi-Fi devices based on the secure digital input/output(SDIO) protocol.

Features:

- SMHC0 controls the devices that comply with the Secure Digital Memory(SD2.0) protocol
- SMHC1 controls the devices that comply with the following protocols:
  - Secure Digital Memory (SD3.0)
  - Secure Digital Input/Output (SDIO 3.0)
- SMHC2 controls the devices that comply with the following protocols:
  - Secure Digital Memory (SD3.0)
  - Multimedia Card (eMMC 5.0/5.1)
- Supports hardware CRC generation and error detection
- Supports host pull-up control
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 1024 bytes FIFO for data transfer

5.3.2. Block Diagram

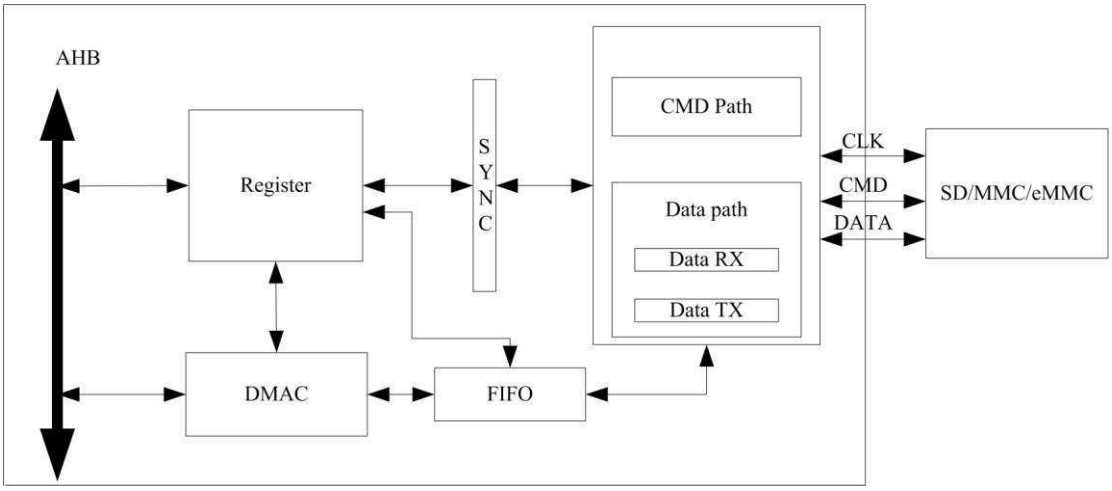


Figure 5-16. SMHC Block Diagram

5.3.3. Operations and Functional Descriptions

5.3.3.1. External Signals

Table 5-3 describes the external signals of SMHC.

Table 5-3. SMHC External Signals

Port Name	Width	Direction	Description
SDC0_CLK	1	O	Clock output for SD/TF card
SDC0_CMD	1	I/O	CMD line for SD/TF card
SDC0_D[i] (i=0~3)	4	I/O	Data line for SD/TF card
SDC1_CLK	1	O	Clock output for SDIO Wi-Fi
SDC1_CMD	1	I/O	CMD line for SDIO Wi-Fi
SDC1_D[i] (i=0~3)	4	I/O	Data line for SDIO Wi-Fi
SDC2_CLK	1	O	Clock output for MMC
SDC2_CMD	1	I/O	CMD line for MMC
SDC2_D[i] (i=0~7)	8	I/O	Data line for MMC
SDC2_RST	1	O	Reset signal for MMC

5.3.3.2. Clock Sources

Each SMHC gets three different clocks. User can select one of them to make SMHC clock source. Table 5-4 describes the clock sources of SMHC. Users can see **CCU** for clock setting, configuration and gating information.

Table 5-4. SMHC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(2X)	Peripheral Clock, the default value is 1.2GHz
PLL_PERIPH1(2X)	Peripheral Clock, the default value is 1.2GHz

5.3.3.3. SMHC Timing Diagram

Please refer to relative specifications:

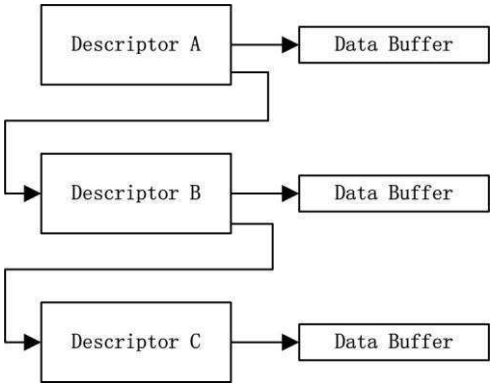
- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver3.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card(eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card(eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard(5.0)

5.3.3.4. Internal DMA Controller Description

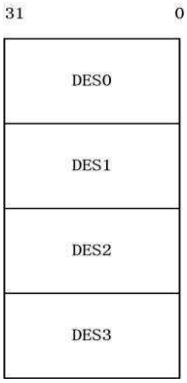
SD/MMC controller has an internal DMA controller (IDMAC) to transfer data between host memory and SDMMC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

5.3.3.4.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.



This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.



DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96] bits in a descriptor.

5.3.3.4.2. DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:6	/	/
5	/	Not used
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

5.3.3.4.3. DES1 Definition

Bits	Name	Descriptor
31:16	/	/
15:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

5.3.3.4.4. DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32.

5.3.3.4.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present.

5.3.3.5. Calibrate Delay Chain

The sample clock delay chain and Data Strobe delay chain(only in SMHC2) are used to generate delay to make proper timing between sample clock/Data Strobe and data signals. Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through **Bus Software Reset Register 0** and **Bus Clock Gating Register0**.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(**CCU**). Calibration delay chain a internal function in SMHC and don't need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200MHz.

Step3: Set proper initial delay value. Writing 0xA0 to ***delay control register*** enables ***Delay Software Enable*** **(bit[7])** and sets initial delay value 0x20 to ***Delay chain*****(bit[5:0])**. Then write 0x0 to ***delay control register*** to clear the value.

Step4: Write 0x8000 to ***delay control register*** to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in ***delay control register***) of calibration done is set. The number of delay cells is shown at Bit8~Bit13 in ***delay control register***. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the cycle of SMHC's clock and the result of calibration.

Note: In the above descriptions,***delay control register*** contains **SMHC Sample Delay Control Register** and **SMHC Data Strobe Delay Control Register.*****Delay Software Enable*** contains **Sample Delay Software Enable** and **Data Strobe Delay Software Enable.** ***Delay chain*** contains **Sample Delay Software** and **Data Strobe Delay Software.**

5.3.4. Register List

Module Name	Base Address
SMHC0	0x01C0F000
SMHC1	0x01C10000

SMHC2	0x01C11000

Register Name	Offset	Description
SMHC_GCTL	0x0000	Control Register
SMHC_CKCR	0x0004	Clock Control Register
SMHC_TMOR	0x0008	Time Out Register
SMHC_BWDR	0x000C	Bus Width Register
SMHC_BKSR	0x0010	Block Size Register
SMHC_BYCR	0x0014	Byte Count Register
SMHC_CMDR	0x0018	Command Register
SMHC_CAGR	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_IMKR	0x0030	Interrupt Mask Register
SMHC_MISR	0x0034	Masked Interrupt Status Register
SMHC_RISR	0x0038	Raw Interrupt Status Register
SMHC_STAR	0x003C	Status Register
SMHC_FWLR	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_A12A	0x0058	Auto Command 12 Argument
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_SDBG	0x0060	SD New Timing Set Debug Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_DMAC	0x0080	BUS Mode Control
SMHC_DLBA	0x0084	Descriptor List Base Address
SMHC_IDST	0x0088	DMAC Status
SMHC_IDIE	0x008C	DMAC Interrupt Enable
SMHC_CHDA	0x0090	Current Host Descriptor Address Register
SMHC_CBDA	0x0094	Current Buffer Descriptor Address Register
SMHC_THLDC	0x0100	Card Threshold Control Register
SMHC_DSBD	0x010C	eMMC4.5 DDR Start Bit Detection Control
SMHC_RES_CRC	0x0110	Response CRC from Device
SMHC_DATA7_CRC	0x0114	CRC Data7 from Card/eMMC
SMHC_DATA6_CRC	0x0118	CRC Data6 from Card/eMMC
SMHC_DATA5_CRC	0x011C	CRC Data5 from Card/eMMC
SMHC_DATA4_CRC	0x0120	CRC Data4 from Card/eMMC
SMHC_DATA3_CRC	0x0124	CRC Data3 from Card/eMMC
SMHC_DATA2_CRC	0x0128	CRC Data2 from Card/eMMC
SMHC_DATA1_CRC	0x012C	CRC Data1 from Card/eMMC
SMHC_DATA0_CRC	0x0130	CRC Data0 from Card/eMMC
SMHC_CRC_STA	0x0134	CRC Status from Device in Write Operation
SMHC_DRV_DL	0x0140	Drive Delay Control Register

SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
SMHC_FIFO	0x0200	Read/Write FIFO

5.3.5. Register Description

5.3.5.1. SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			**Register Name: SMHC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 0: DMA bus 1: AHB bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in **DTO_LMT**. 0: 1card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable

			0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

5.3.5.2. SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: SMHC_CLKDIV**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off

			1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card Clock Divider n: Source clock is divided by 2*n.(n=0~255)

5.3.5.3. SMHC Timeout Register (Default Value: 0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

5.3.5.4. SMHC Bus Width Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

5.3.5.5. SMHC Block Size Register (Default Value: 0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

5.3.5.6. SMHC Block Count Register (Default Value: 0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte Counter

			Number of bytes to be transferred. It should be integer multiple of Block Size for block transfers.

5.3.5.7. SMHC Command Register (Default Value: 0x0000_0000)

Offset: 0x0018			**Register Name: SMHC_CMD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command. This bit is automatically cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: Normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, the controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock. When this bit is set, the controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ

			Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48-bit) 1: Long Response (136-bit)

6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

5.3.5.8. SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command Argument

5.3.5.9. SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

5.3.5.10. SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

5.3.5.11. SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

5.3.5.12. SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

5.3.5.13. SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN

			Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

5.3.5.14. SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			**Register Name: SMHC_MINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	M_CARD_REMOVAL_INT Card Removed
30	R/W	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R/W	0x0	M_SDIO_INT SDIO Interrupt
15	R/W	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R/W	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R/W	0x0	M_DSE_BC_INT Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared.
12	R/W	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R/W	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R/W	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R/W	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R/W	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R/W	0x0	M_DCE_INT Data CRC Error

			When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R/W	0x0	M_RCE_INT Response CRC Error
5	R/W	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R/W	0x0	M_DTR_INT Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data.
3	R/W	0x0	M_DTC_INT Data Transfer Complete
2	R/W	0x0	M_CC_INT Command Complete
1	R/W	0x0	M_RE_INT Response Error (no response or response CRC error) When set, Transmit Bit error or End Bit error or CMD Index error may occur.
0	/	/	/

5.3.5.15. SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: SMHC_RINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bit.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bit.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bit.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bit.
14	R/W1C	0x0	ACD

			Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bit.
13	R/W1C	0x0	DSE_BC Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared. This is write-1-to-clear bit.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bit.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bit.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bit.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start This is write-1-to-clear bit.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bit.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bit.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bit.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bit.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. This is write-1-to-clear bit.
3	R/W1C	0x0	DTC Data Transfer Complete

			This is write-1-to-clear bit.
2	R/W1C	0x0	CC Command Complete This is write-1-to-clear bit.
1	R/W1C	0x0	RE Response Error (no response or response CRC error) When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bit.
0	/	/	/

5.3.5.16. SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			**Register Name: SMHC_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card Data Busy Inverted version of DATA[0] 0: Card data not busy 1: Card data busy
8	R	0x0	CARD_PRESENT Data[3] Status Level of DATA[3]; checks whether card is present 0: Card not present 1: Card present
7:4	R	0x0	FSM_STA Command FSM States 0000: Idle 0001: Send init sequence

			0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO Full 0: FIFO not full 1: FIFO full
2	R	0x1	FIFO_EMPTY FIFO Empty 0: FIFO not empty 1: FIFO empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach receive trigger level 1: FIFO reached receive trigger level

5.3.5.17. SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			**Register Name: SMHC_FIFOTH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers

			001: 4 010: 8 011: 16 (only SMHC2 support) Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: MSize = 16, TX_TL = 240, RX_TL = 15(SMHC2)
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF: Reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15)(SMHC2)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: No trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)(SMHC2)

5.3.5.18. SMHC Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: SMHC_FUNS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data

			0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets the bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

5.3.5.19. SMHC Transferred Byte Count Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			**Register Name: SMHC_TBC_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.5.20. SMHC Transferred Byte Count Register1 (Default Value: 0x0000_0000)

Offset: 0x004C			**Register Name: SMHC_TBC_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.5.21. SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	SMHC_A12A. SMHC_A12A set the argument of command 12 automatically send by controller

5.3.5.22. SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock , command and data RX phase clear 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, data RX phase clear 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data , data RX phase clear 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data , data RX phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command RX phase clear

			0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE(RX) 00: Sample timing phase offset 90° 01: Sample timing phase offset 180° 10: Sample timing phase offset 270° 11: Ignore
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE(RX) 00: Sample timing phase offset 90° 01: Sample timing phase offset 180° 10: Sample timing phase offset 270° 11: Ignore
3:0	/	/	/

Note: This register is for SMHC0 ,SMHC1 only.

5.3.5.23. SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			**Register Name: SMHC_HWRST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST. 0: Reset 1: Active mode These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

5.3.5.24. SMHC DMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			**Register Name: SMHC_DMAC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	PRG_BURST_LEN

			Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows. 000: 1 transfers 001: 4 transfers 010: 8 transfers 011: 16 transfers Transfer unit is 32 bits. PBL is a read-only value.
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0x0	DES_SKIP_LEN Descriptor Skip Length. Specifies the number of Word to skip between two unchained descriptors. This is applicable only for dual buffer structure. Default value is set to 4 DWORD.
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

5.3.5.25. SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			**Register Name: SMHC_DLBA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bit[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

5.3.5.26. SMHC DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_DST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	DMAC_FSM_STA DMAC FSM Present State. 0000: DMA_IDLE 0001: DMA_SUSPEND 0010: DESC_RD 0011: DESC_CHK 0100: DMA_RD_REQ_WAIT 0101: DMA_WR_REQ_WAIT 0110: DMA_RD 0111: DMA_WR 1000: DESC_CLOSE
12:10	R	0x0	DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (**FATAL_BERR_INT**) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved EB is read-only.
9	R/W1C	0x0	ABN_INT_SUM Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: DU bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM Normal Interrupt Summary. Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/

5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (**DMAC_ERR_STA**). When this bit is set, the DMA disables all its bus accesses. Writing a '1' clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a '1' clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit.

5.3.5.27. SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			**Register Name: SMHC_IDIE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	ABN_INT_ENB Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: IDINTEN[2]: Fatal Bus Error Interrupt IDINTEN[4]: DU Interrupt

			IDINTEN[5]: Card Error Summary Interrupt
8	R/W	0x0	NOR_INT_ENB Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: IDINTEN[0]: Transmit Interrupt IDINTEN[1]: Receive Interrupt
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

5.3.5.28. SMHC Current Host Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			**Register Name: SMHC_CHDA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_DES_ADDR Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC.

5.3.5.29. SMHC Current Buffer Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0094	**Register Name: SMHC_CBDA_REG**

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_BUFF_ADDR Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC.

5.3.5.30. SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_RD_THLD Card Read Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB (only for SMHC2) Card Write Threshold Enable(HS400) 0: Card Write Threshold Disable 1: Card Write Threshold Enable Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO.
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy Clear Interrupt Disable 1: Busy Clear Interrupt Enable The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if **CARD_RD_THLD** amount of space is available in receive FIFO.

5.3.5.31. SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: SMHC_EDSD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable It is required to set **HS400_MD_EN** to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set **HALF_START_BIT** to 1 for eMMC 4.5 and above; set to 0 for SD applications.

5.3.5.32. SMHC Response CRC Register (Default Value: 0x0000_0000)

Offset: 0x0110			**Register Name: SMHC_RESP_CRC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device.

Note: This register is for SMHC0, SMHC1 only.

5.3.5.33. SMHC Data7 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0114			**Register Name: SMHC_DATA7_CRC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT7_CRC Data[7] CRC CRC in data[7] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.34. SMHC Data6 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: SMHC_DATA6_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT6_CRC Data[6] CRC CRC in data[6] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.35. SMHC Data5 CRC Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SMHC_DATA5_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT5_CRC Data[5] CRC CRC in data[5] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.36. SMHC Data4 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: SMHC_DATA4_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT4_CRC Data[4] CRC CRC in data[4] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode,the higher 16-bit indicates the CRC of odd data, ,and the lower 16-bit indicates the CRC of even data. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.37. SMHC Data3 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: SMHC_DATA3_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT3_CRC Data[3] CRC CRC in data[3] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode,the higher 16-bit indicates the CRC of odd data, ,and the lower 16-bit indicates the CRC of even data. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.38. SMHC Data2 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: SMHC_DATA2_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT2_CRC Data[2] CRC CRC in data[2] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode,the higher 16-bit indicates the CRC of odd data, ,and the lower 16-bit indicates the CRC of even data. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.39. SMHC Data1 CRC Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: SMHC_DATA1_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT1_CRC Data[1] CRC CRC in data[1] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode,the higher 16-bit indicates the CRC of odd data, ,and the lower 16-bit indicates the CRC of even data. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.40. SMHC Data0 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: SMHC_DATA0_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT0_CRC Data[0] CRC CRC in data[0] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode,the higher 16-bit indicates the CRC of odd data, ,and the lower 16-bit indicates the CRC of even data. In SDR mode, the higher 16-bit indicates the CRC of all data.

Note: This register is for SMHC0,SMHC1 only.

5.3.5.41. SMHC CRC Status Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: SMHC_CRC_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	CRC_STA CRC Status CRC status from device in write operation 010: Positive CRC status token 101: Negative CRC status token

Note: This register is for SMHC0,SMHC1 only.

5.3.5.42. SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Drive phase offset is 90^0 1: Drive phase select is 180^0 In DDR mode, only 90^0 phase offset is valid.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Drive phase offset is 90^0

			1: Drive phase select is 180^0
15:0	/	/	/

5.3.5.43. SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in **SAMP_DL**.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when **SAMP_DL_CAL_DONE** is set.
7	RW	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at **SAMP_DL_SW**.
6	/	/	/
5:0	RW	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of **SAMP_DL**, the cycle of card clock and device's input timing requirement.

5.3.5.44. SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	RW	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done

			When set, it means that sample delay chain calibration is done and the result of calibration is shown in **DS_DL**.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when **SAMP_DL_CAL_DONE** is set.
7	RW	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	RW	0x0	DS_DL_SW Data Strobe Delay Software

Note: This register is for SMHC2 only.

5.3.5.45. SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			**Register Name: SMHC_FIFO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

Chapter 6 Image

This section describes the image input of H5:

- CSI

6.1. CSI

6.1.1. Overview

The CSI includes the following feature:

CSI

- Supports 8-bit yuv422 CMOS sensor interface
- Supports CCIR656 protocol for NTSC and PAL
- Maximum still capture resolution to 5M
- Maximum video capture resolution to 1080@30fps

CCI

- Compatible with I2C transmission in 7-bit slave ID and 1-bit R/W
- Automatic transmission
- 0/8/16/32-bit register address supported
- 8/16/32-bit data supported
- 64 bytes FIFO input CCI data supported
- Synchronized with CSI signal and delay trigger supported
- Repeated transmission with sync signal supported

6.1.2. Block Diagram

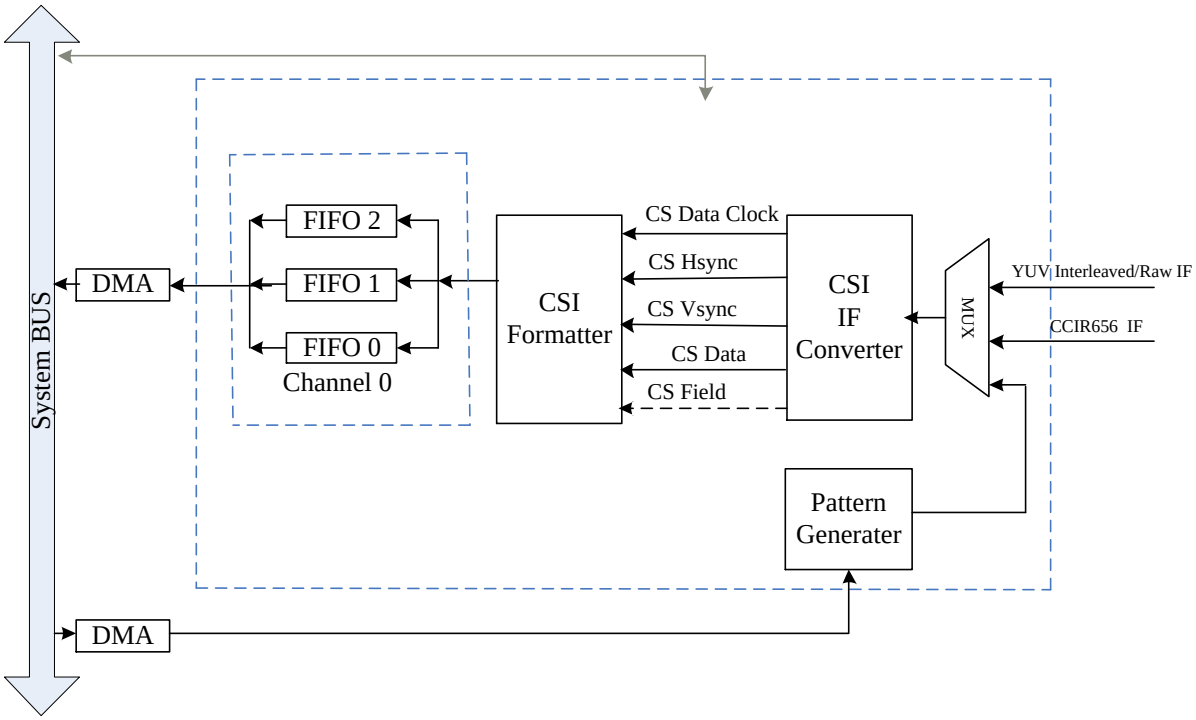


Figure 6-1. CSI Block Diagram

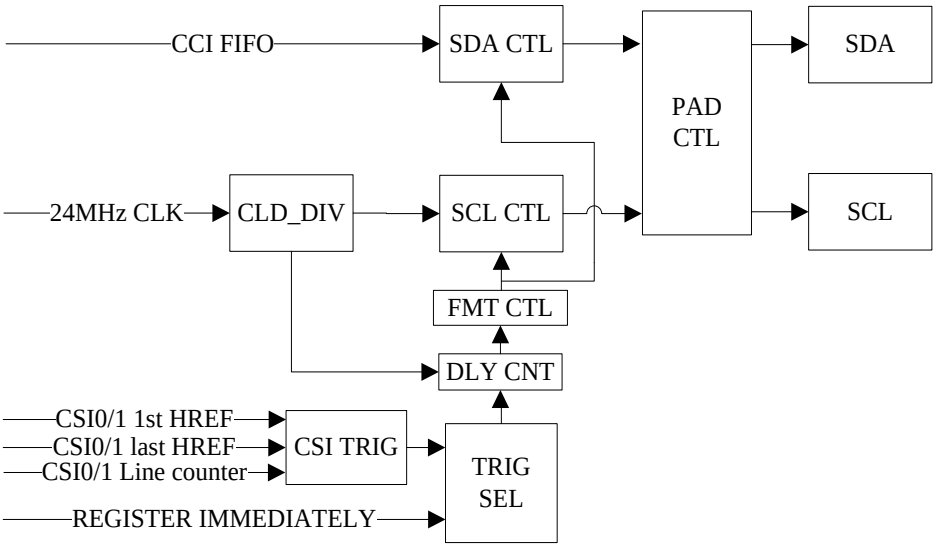


Figure 6-2. CCI Block Diagram

6.1.3. Operations and Functional Descriptions

6.1.3.1. CSI FIFO Distribution

Table 6-1. CSI FIFO Distribution

Interface	YUYV422 Interleaved/Raw			BT656 Interface	
Input format	YUV422		Raw	YUV422	
Output format	Planar	UV combined/ MB	Raw/RGB/PRGB	Planar	UV combined/MB
CH0_FIFO0	Y pixel data	Y pixel data	All pixels data	Y	Y
CH0_FIFO1	Cb (U) pixel data	Cb (U) Cr (V) pixel data	-	Cb (U)	CbCr (UV)
CH0_FIFO2	Cr (V) pixel data	-	-	Cr (V)	

6.1.3.2. CSI Timing

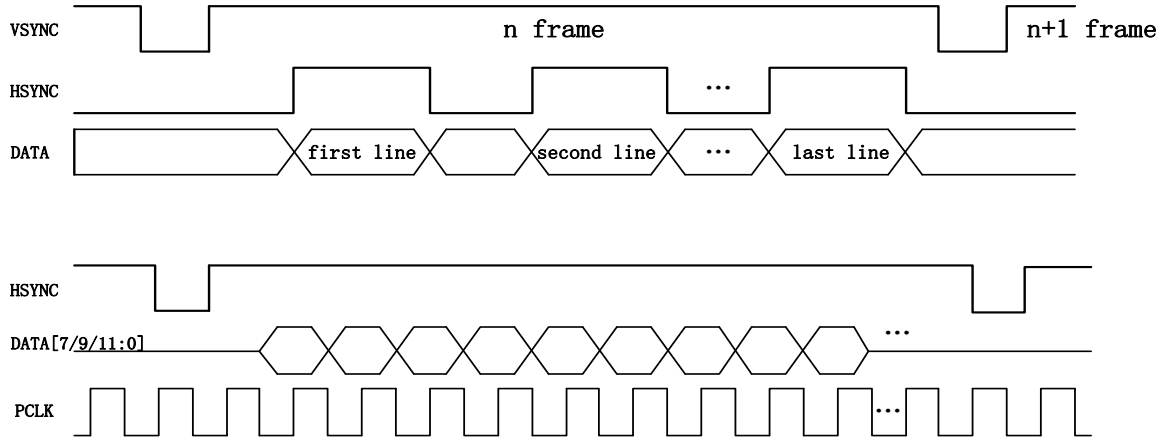


Figure 6-3. 8/10/12-bit CMOS Sensor Interface Timing

(clock rising edge sample.vsync valid = positive,hsycn valid = positive)

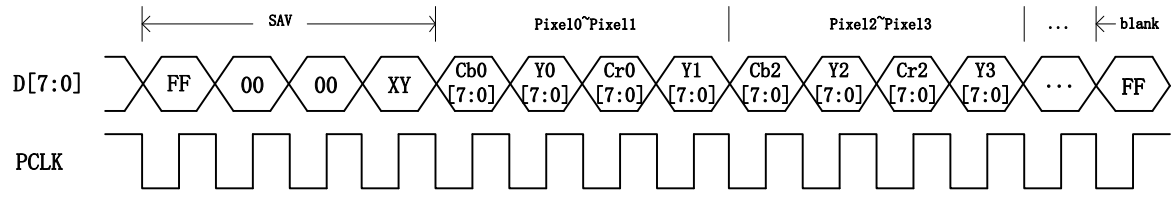


Figure 6-4. 8-bit YCbCr4:2:2 with Embedded Syncs(BT656) Timing

6.1.3.3. Bit Definition

CCIR656 Header Data Bit Definition:

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	1	0	0	1
CS D[8]	1	0	0	F
CS D[7]	1	0	0	V
CS D[6]	1	0	0	H
CS D[5]	1	0	0	P3
CS D[4]	1	0	0	P2
CS D[3]	1	0	0	P1
CS D[2]	1	0	0	P0
CS D[1]	x	x	x	x
CS D[0]	x	x	x	x

Note: For compatibility with 8-bit interface, CS D[1] and CS D[0] are not defined.

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

6.1.4. Register list

Module Name	Base Address
CSI0	0x01CB0000

Register Name	Offset	Register name
CSI0_EN_REG	0x0000	CSI Enable Register
CSI0_IF_CFG_REG	0x0004	CSI Interface Configuration Register
CSI0_CAP_REG	0x0008	CSI Capture Register
CSI0_SYNC_CNT_REG	0x000C	CSI Synchronization Counter Register
CSI0_FIFO_THRS_REG	0x0010	CSI FIFO Threshold Register
CSI0_PTN_LEN_REG	0x0030	CSI Pattern Generation Length Register
CSI0_PTN_ADDR_REG	0x0034	CSI Pattern Generation Address Register
CSI0_VER_REG	0x003C	CSI Version Register
CSI0_C0_CFG_REG	0x0044	CSI Channel_0 Configuration Register
CSI0_C0_SCALE_REG	0x004C	CSI Channel_0 Scale Register

CSI0_C0_F0_BUFA_REG	0x0050	CSI Channel_0 FIFO 0 Output Buffer-A Address Register
CSI0_C0_F1_BUFA_REG	0x0058	CSI Channel_0 FIFO 1 Output Buffer-A Address Register
CSI0_C0_F2_BUFA_REG	0x0060	CSI Channel_0 FIFO 2 Output Buffer-A Address Register
CSI0_C0_CAP_STA_REG	0x006C	CSI Channel_0 Status Register
CSI0_C0_INT_EN_REG	0x0070	CSI Channel_0 Interrupt Enable Register
CSI0_C0_INT_STA_REG	0x0074	CSI Channel_0 Interrupt Status Register
CSI0_C0_HSIZE_REG	0x0080	CSI Channel_0 Horizontal Size Register
CSI0_C0_VSIZE_REG	0x0084	CSI Channel_0 Vertical Size Register
CSI0_C0_BUF_LEN_REG	0x0088	CSI Channel_0 Line Buffer Length Register
CSI0_C0_FLIP_SIZE_REG	0x008C	CSI Channel_0 Flip Size Register
CSI0_C0_FRM_CLK_CNT_REG	0x0090	CSI Channel_0 Frame Clock Counter Register
CSI0_C0_ACC_ITNL_CLK_CNT_REG	0x0094	CSI Channel_0 Accumulated and Internal Clock Counter Register
CSI0_C0_FIFO_STAT_REG	0x0098	CSI Channel_0 FIFO Statistic Register
CSI0_C0_PCLK_STAT_REG	0x009C	CSI Channel_0 PCLK Statistic Register
CCI_CTRL	0x3000	CCI Control Register
CCI_CFG	0x3004	CCI Transmission Configuration Register
CCI_FMT	0x3008	CCI Packet Format Register
CCI_BUS_CTRL	0x300C	CCI Bus Control Register
CCI_INT_CTRL	0x3014	CCI Interrupt Control Register
CCI_LC_TRIG	0x3018	CCI Line Counter Trigger Register
CCI_FIFO_ACC	0x3100	CCI FIFO Access Register
CCI_RSV_REG	0x3200	CCI Reserved Register

6.1.5. Register Description

6.1.5.1. CSI Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: CSI0_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	VER_EN CSI Version Register Read Enable 0: Disable 1: Enable
29:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:9	/	/	/
8	R/W	0x0	SRAM_PWDN

			0: SRAM in normal 1: SRAM in power down
7:5	/	/	/
4	R/W	0x0	PTN_START CSI Pattern Generating Start 0: Finish 1: Start Software writes this bit to“1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to “0” automatically. Generating cycles depends on PTN_CYCLE.
3	R/W	0x0	CLK_CNT_SPL Sampling time for CLK counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
2	R/W	0x0	CLK_CNT_EN CLK count per frame enable
1	R/W	0x0	PTN_GEN_EN Pattern Generation Enable
0	R/W	0x0	CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module

6.1.5.2. CSI Interface Configuration Register (Default Value: 0x0005_0000)

Offset: 0x0004			**Register Name: CSI0_IF_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	SRC_TYPE Source Type 0: Progressed 1: Interlaced
20	R/W	0x0	FPS_DS Fps Down Sample 0: No down sample 1: 1/2 fps, only receives the first frame every 2 frames
19	R/W	0x0	FIELD For YUV HV timing, Field polarity

			0: Negative(field=0 indicate odd, field=1 indicate even) 1: Positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref Polarity 0: Negative 1: Positive The bit does not apply for CCIR656 interface.
17	R/W	0x0	HERF_POL Href Polarity 0: Negative 1: Positive The bit does not apply for CCIR656 interface.
16	R/W	0x1	CLK_POL Data Clock Type 0: Active in rising edge 1: Active in falling edge
15:12	/	/	/
11:10	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual csi data bus according to these sequences 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
9:8	R/W	0x0	IF_DATA_WIDTH 00: 8 bits data bus 01: 10 bits data bus 10: 12 bits data bus 11: 8+2 bits data bus
7:5	/	/	/
4:0	R/W	0x0	CSI_IF YUV:

			00000: YUYV422 Interleaved or RAW (All data in one data bus) CCIR656: 00100: YUYV422 Interleaved or RAW (All data in one data bus) Others: Reserved

6.1.5.3. CSI Capture Register (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: CSI0_CAP_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:2	R/W	0x0	CH0_CAP_MASK Vsync number masked before capture.
1	R/W	0x0	CH0_VCAP_ON Video capture control: capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/W	0x0	CH0_SCAP_ON Still capture control: capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

6.1.5.4. CSI Synchronization Counter Register (Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: CSI0_SYNC_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	SYNC_CNT The counter value between vsync of CSI0 channel 0 and vsync of CSI1 channel 0 , using 24MHz.

6.1.5.5. CSI FIFO Threshold Register (Default Value: 0x040F_0400)

Offset: 0x0010			Register Name: CSI0_FIFO_THRS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:26	R/W	0x1	FIFO_NEARLY_FULL_TH The threshold of FIFO being nearly full. Indicates that the ISP should stop writing. Only valid when ISP is enabled. The smaller the value of the field, the flag of FIFO being nearly full is easier to reach.
25:24	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
23:16	R/W	0x0f	PTN_GEN_DLY Clocks delayed before pattern generating start.
15:12	/	/	/
11:00	R/W	0x400	FIFO_THRS When CSI0 FIFO occupied memory exceed the threshold, dram frequency can not change.

6.1.5.6. CSI Pattern Generation Length Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CSI0_PTN_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

6.1.5.7. CSI Pattern Generation Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CSI0_PTN_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

6.1.5.8. CSI Version Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CSI0_VER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	VER Version of hardware circuit. Only can be read when version register read enable is on.

6.1.5.9. CSI Channel_0 Configuration Register (Default Value: 0x0030_0200)

Offset: 0x0044			Register Name: CSI0_C0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888
23:20	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: Reserved 0010: Reserved 0011: YUV422 0100: YUV420 Others: Reserved
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420

			1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: Capturing with field 1. 01: Capturing with field 2. 10: Capturing with either field. 11: Reserved
9:8	R/W	0x2	INPUT_SEQ

			Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
7:2	/	/	/
1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if hflip is enabled, always select 256 bytes) 1: 512 bytes 2: 1K bytes 3: 2K bytes

6.1.5.10. CSI Channel_0 Scale Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CSI0_C0_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

6.1.5.11. CSI Channel_0 FIFO 0 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CSI0_C0_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	C0F0_BUFA FIFO 0 output buffer-A address

6.1.5.12. CSI Channel_0 FIFO 1 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CSI0_C0_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	C0F1_BUFA FIFO 1 output buffer-A address

6.1.5.13. CSI Channel_0 FIFO 2 Output Buffer-A Address Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: CSI0_C0_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	C0F2_BUFA FIFO 2 output buffer-A address

6.1.5.14. CSI Channel_0 Status Register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: CSI0_C0_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.5.15. CSI Channel_0 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: CSI0_C0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	VS_INT_EN Vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after the IRQ come, change the buffer address could only effect next frame.

6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data is written to buffer. For video capture, the bit is set when the last frame is written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.16. CSI Channel_0 Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0074			**Register Name: CSI0_C0_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	VS_PD Vsync flag
6	R/W	0x0	HB_OF_PD Hblank FIFO overflow
5	R/W	0x0	MUL_ ERR_PD Multi-channel writing error
4	R/W	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W	0x0	FIFO1_OF_PD FIFO 1 overflow

2	R/W	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W	0x0	FD_PD Frame done
0	R/W	0x0	CD_PD Capture done

6.1.5.17. CSI Channel_0 Horizontal Size Register (Default Value: 0x0500_0000)

Offset: 0x0080			**Register Name: CSI0_C0_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.1.5.18. CSI Channel_0 Vertical Size Register (Default Value: 0x01E0_0000)

Offset: 0x0084			**Register Name: CSI0_C0_VSIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

6.1.5.19. CSI Channel_0 Buffer Length Register (Default Value: 0x0140_0280)

Offset: 0x0088			**Register Name: CSI0_C0_BUF_LEN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:14	/	/	/
13:0	R/W	0x280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

6.1.5.20. CSI Channel_0 Flip Size Register (Default Value: 0x01E0_0280)

Offset: 0x008C			Register Name: CSI0_C0_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	0x280	VALID_LEN Valid components of a line when in flip mode.

6.1.5.21. CSI Channel_0 Frame Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: CSI0_C0_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:00	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by 1 every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to **FRM_CLK_CNT**, and cleared to 0.

6.1.5.22. CSI Channel_0 accumulated and internal clock counter Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: CSI0_C0_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ACC_CLK_CNT The accumulated value of **FRM_CLK_CNT** for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clears it to 0. If the **ACC_CLK_CNT** is larger than 1, the software has lost frame. When frame done or vsync comes, **ACC_CLK_CNT** = **ACC_CLK_CNT** + 1, and cleared to 0 when writing 0 to this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame-done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.1.5.23. CSI Channel_0 FIFO Statistic Register (Default Value: 0x0000_0000)

Offset: 0x0098	Register Name: CSI0_C0_FIFO_STAT_REG

Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or frame-done.

6.1.5.24. CSI Channel_0 PCLK Statistic Register (Default Value: 0x0000_7FFF)

Offset: 0x009C			Register Name: CSI0_C0_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or frame-done.
15	/	/	/
14:00	R	0x7fff	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or frame-done.

6.1.5.25. CCI Control Register (Default Value: 0x0000_0000)

Offset: 0x3000			Register Name: CCI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SINGLE_TRAN 0: Transmission idle 1: Start single transmission Automatically cleared to '0' when finished. Abort current transmission immediately if changing from '1' to '0'. If slave does not respond for the expected status over the time defined by TIMEOUT, the current transmission will stop. **PACKET_CNT** will return the sequence number when transmission failed. All format setting and data will be loaded from registers and FIFO when transmission started.
30	R/W	0x0	REPEAT_TRAN 0: Transmission idle 1: Repeated transmission When this bit is set to 1, transmission repeats when trigger signal (such as VSYNC/ VCAP done) repeats. If changing this bit from '1' to '0' during transmission, the current transmission will be guaranteed then stop.

29	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the CCI action after sent register address.
28	R/W	0x0	READ_TRAN_MODE 0: Send slave_id+W 1: Do not send slave_id+W **Note:** Setting this bit to 1 if reading from a slave which register width is equal to 0.
27:24	R	0x0	TRAN_RESULT 000: OK 001: FAIL Other: Reserved
23:16	R	/	CCI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:2	/	/	/
1	R/W	0x0	SOFT_RESET 0: Normal 1: Reset
0	R/W	0x0	CCI_EN 0: Module disable 1: Module enable

6.1.5.26. CCI Transmission Configuration Register (Default Value: 0x1000_0000)

Offset: 0x3004			Register Name: CCI_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device does not response after N*FSCL cycles. And software must reset CCI module and send a stop condition to slave.
23:16	R/W	0x0	INTERVAL Define the interval between each packet in 40*FSCL cycles.
15	R/W	0x0	PACKET_MODE Select where to load slave id / data width 0: Compact mode 1: Complete mode In compact mode, slave id/register width/data width will be loaded from CCI_FMT register, only address and data read from memory. In complete mode, they will be loaded from packet memory.
14:7	/	/	/
6:4	R/W	0x0	TRIG_MODE Transmit mode 000: Immediately, no trigger 001: Reserved 010: CSI0 int trigger 011: CSI1 int trigger
3:0	R/W	0x0	CSI_TRIG CSI Int trig signal select 0000: First HREF start 0001: Last HREF done 0010: Line counter trigger other: Reserved

6.1.5.27. CCI Packet Format Register (Default Value: 0x0011_0001)

Offset: 0x3008			Register Name: CCI_FMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	SLV_ID 7bit address
24	R/W	0x0	CMD 0: write

			1: read
23:20	R/W	0x1	ADDR_BYTE How many bytes be sent as address 0~15
19:16	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~15 Normally use ADDR_DATA with 0_2, 1_1, 1_2, 2_1, 2_2 access mode. If DATA byte is 0, transmission will not start. In complete mode, the **ADDR_BYTE** and **DATA_BYTE** are defined in the high/low 4bit of a byte.
15:0	R/W	0x1	PACKET_CNT FIFO data is transmitted as PACKET_CNT packets in current format. Total bytes must not exceed 32bytes.

6.1.5.28. CCI Bus Control Register (Default Value: 0x0000_2500)

Offset: 0x300C			**Register Name: CCI_BUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	DLY_CYC 0~65535 FSCL cycles between each transmission
15	R/W	0x0	DLY_TRIG 0: Disable 1: Execute transmission after internal counter delay when triggered
14:12	R/W	0x2	CLK_N CCI bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x5	CLK_M CCI output SCL frequency is FSCL=F1/10=(F0/(CLK_M+1))/10
7	R	/	SCL_STA SCL current status
6	R	/	SDA_STA SDA current status
5	R/W	0x0	SCL_PEN SCL PAD enable
4	R/W	0x0	SDA_PEN SDA PAD enable
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE

			SDA manual output en

6.1.5.29. CCI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x3014			Register Name: CCI_INT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	S_TRAN_ERR_INT_EN
16	R/W	0x0	S_TRAN_COM_INT_EN
15:2	/	/	/
1	R/W	0x0	S_TRAN_ERR_PD
0	R/W	0x0	S_TRAN_COM_PD

6.1.5.30. CCI Line Counter Trigger Control Register (Default Value: 0x0000_0000)

Offset: 0x3018			Register Name: CCI_LC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LN_CNT 0~8191: Line counter send trigger when 1st~8192th line is received.

6.1.5.31. CCI FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x3100~0x313F			Register Name: CCI_FIFO_ACC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA_FIFO From 0x3100 to 0x313f, CCI data FIFO is 64 bytes, used in FIFO input mode. CCI transmission read/write data from/to FIFO in byte.

Chapter 7 Display

This chapter describes the H5 display system from following perspectives:

- DE2.0
- TCON

The following figure shows the block diagram of display system:

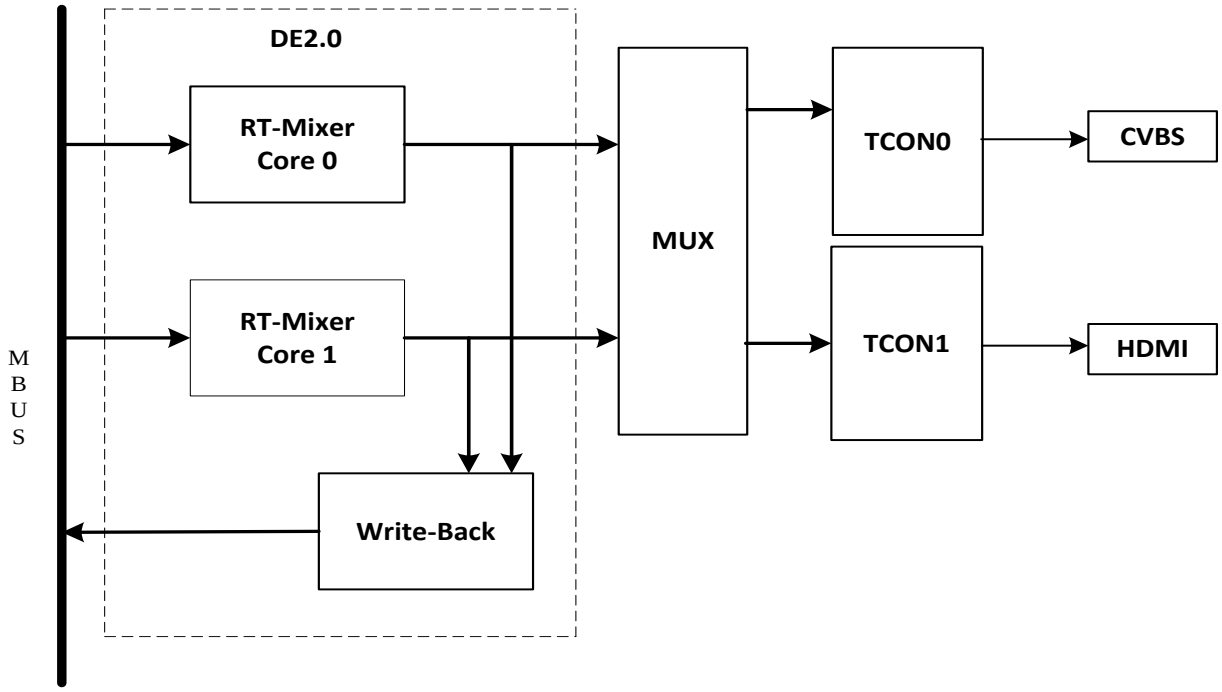


Figure 7-1. Display System Block Diagram

7.1. DE2.0

7.1.1. Overview

The Display Engine 2.0(DE2.0) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE2.0 supports four overlay windows to blend, and supports image post-processing in the video channel.

Features:

- Output size up to 4096x4096
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor 2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports writeback for high efficient dual display and miracast

7.2. TCON

7.2.1. Overview

The TCON0 module is used for LCD, and TCON1 module is used for TV.

- Supports HDMI interface, up to 1080p
- Supports TV interface, up to 480p/576p
- 2 interrupts for programmer single TCON output

7.2.2. Block Diagram

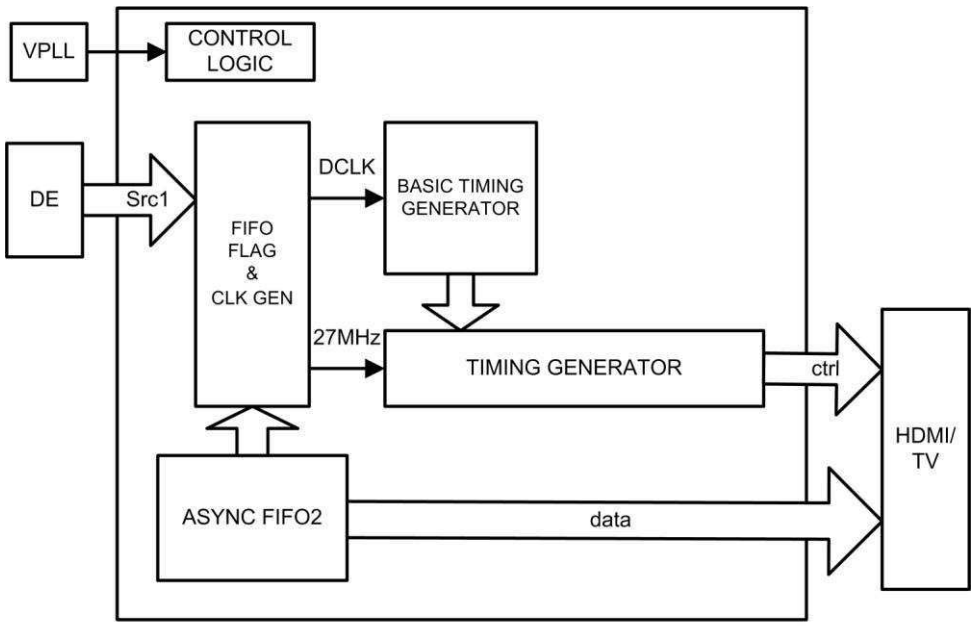


Figure 7-2. TCON Block Diagram

7.2.3. Operations and Functional Descriptions

7.2.3.1. RGB Gamma Correction

Function: This module correct the RGB input data of DE .

A 256*8*3 Byte register file is used to store the gamma table. The following is the layout:

Offset	Value
0x400, 0x401, 0x402	{ B0[7:0], G0[7:0], R0[7:0] }

0x404,	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x4FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.2.3.2. CEU Module

Function: This module enhance color data from DE .

R' = Rr*R + Rg*G + Rb*B + Rc

G' = Gr*R + Gg*G + Gb*B +Gc

B' = Br*R + Bg*G + Bb*B + Bc

Note:

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb s13(-16,16)

Rc, Gc, Bc s19 (-16384, 16384)

R, G, B u8 [0-255]

R' have the range of [Rmin ,Rmax]

G' have the range of [Rmin ,Rmax]

B' have the range of [Rmin ,Rmax]

7.2.4. TCON0 Module Register List

Module Name	Base Address
TCON0	0x01C0C000

Register Name	Offset	Description
TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON1_CTL_REG	0x0090	TCON1 Control Register
TCON1_BASIC0_REG	0x0094	TCON1 Basic Timing Register0
TCON1_BASIC1_REG	0x0098	TCON1 Basic Timing Register1
TCON1_BASIC2_REG	0x009C	TCON1 Basic Timing Register2
TCON1_BASIC3_REG	0x00A0	TCON1 Basic Timing Register3
TCON1_BASIC4_REG	0x00A4	TCON1 Basic Timing Register4
TCON1_BASIC5_REG	0x00A8	TCON1 Basic Timing Register5
TCON1_PS_SYNC_REG	0x00B0	TCON1 Sync Register
TCON1_IO_POL_REG	0x00F0	TCON1 IO Polarity Register
TCON1_IO_TRI_REG	0x00F4	TCON1 IO Trigger Register
TCON_ECC_FIFO_REG	0x00F8	TCON ECC FIFO Register
TCON_CEU_CTL_REG	0x0100	TCON CEU Control Register
TCON_CEU_COEF_MUL_REG	0x0110+N*0x04	TCON CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
TCON_CEU_COEF_ADD_REG	0x011C+N*0x10	TCON CEU Coefficient Register1(N=0,1,2)
TCON_CEU_COEF_RANG_REG	0x0140+N*0x04	TCON CEU Coefficient Register2(N=0,1,2)

TCON_SAFE_PERIOD_REG	0x01F0	TCON Safe Period Register
TCON1_FILL_CTL_REG	0x0300	TCON1 Fill Data Control Register
TCON1_FILL_BEGIN_REG	0x0304+N*0x0C	TCON1 Fill Data Begin Register(N=0,1,2)
TCON1_FILL_END_REG	0x0308+N*0x0C	TCON1 Fill Data End Register(N=0,1,2)
TCON1_FILL_DATA0_REG	0x030C+N*0x0C	TCON1 Fill Data Value Register(N=0,1,2)
TCON1_GAMMA_TABLE_REG	0x0400-0x07FF	
TCON_ECC_FIFO_BIST_REG	0x0FFC	

7.2.5. TCON0 Module Register Description

7.2.5.1. TCON Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: TCON_GCTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON_EN 0: Disable 1: Enable When it's disabled, the module will be reset to idle state.
30	R/W	0x0	TCON_GAMMA_EN 0: Disable 1: Enable
29:0	/	/	/

7.2.5.2. TCON Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: TCON_GINT0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TCON1_VB_INT_EN 0: Disable 1: Enable
29	/	/	/
28	R/W	0x0	TCON1_LINE_INT_EN 0: Disable 1: Enable
27:15	/	/	/
14	R/W	0x0	TCON1_VB_INT_FLAG

			Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TCON1_LINE_INT_FLAG Trigger when SY1 match the current TCON1 scan line Write 0 to clear it.
11:0	/	/	/

7.2.5.3. TCON Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: TCON_GINT1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	TCON1_LINE_INT_NUM Scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger1. **Note:** SY1 is writable only when LINE_TRG1 disable.

7.2.5.4. TCON1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0090			**Register Name: TCON1_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON1_EN 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0x0	START_DELAY This is for DE1 and DE2
3:2	/	/	/
1	R/W	0x0	TCON1_SRC_SEL 0: Reserved 1: BLUE data(FIFO2 disable, RGB=0000FF)
0	/	/	/

7.2.5.5. TCON1 Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0094			**Register Name: TCON1_BASIC0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON1_XI

			Source width is X+1
15:12	/	/	/
11:0	R/W	0x0	TCON1_YI Source height is Y+1

7.2.5.6. TCON1 Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TCON1_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO Width is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO Width is LS_YO+1 **Note:** This version LS_YO = TCON1_YI

7.2.5.7. TCON1 Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TCON1_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON1_XO Width is TCON1_XO+1
15:12	/	/	/
11:0	R/W	0x0	TCON1_YO Height is TCON1_YO+1

7.2.5.8. TCON1 Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TCON1_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch Thbp = (HBP +1) * Thdclk

7.2.5.9. TCON1 Basic Timing Register4 (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TCON1_BASIC4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT Horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0x0	VBP Horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

7.2.5.10. TCON1 Basic Timing Register5 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TCON1_BASIC5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk **Note:** HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th **Note:** VT/2 > (VSPW+1)

7.2.5.11. TCON1 SYNC Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: TCON1_PS_SYNC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SYNC_X
15:0	R/W	0x0	SYNC_Y

7.2.5.12. TCON1 IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: TCON1_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV

			0: Not invert 1: Invert
26	R/W	0x0	IO2_INV 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert
23:0	R/W	0x0	DATA_INV TCON output port D[23:0] polarity control, with independent bit control 0s: Normal polarity 1s: Invert the specify output

7.2.5.13. TCON1 IO Trigger Register (Default Value: 0x0FFF_FFFF)

Offset: 0x00F4			**Register Name: TCON1_IO_TRI_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 0: Enable 1: Disable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 0: Enable 1: Disable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 0: Enable 1: Disable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 0: Enable 1: Disable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN TCON output port D[23:0] output enable,with independent bit control.

			0s: Enable 1s: Disable

7.2.5.14. TCON ECC FIFO Register (Default Value: UDF)

Offset: 0x00F8			Register Name: TCON_ECC_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	UDF	ECC_FIFO_BIST_EN 0: Disable 1: Enable
30	R/W	UDF	ECC_FIFO_ERR_FLAG
29:24	/	/	/
23:16	R/W	UDF	ECC_FIFO_ERR_BITS
15:9	/	/	/
8	R/W	UDF	ECC_FIFO_BLANK_EN 0: Disable ECC function in blanking 1: Enable ECC function in blanking ECC function is tent to trigger in blanking area at hv mode, set '0' when in hv mode.
7:0	R/W	UDF	ECC_FIFO_SETTING Bit3 0: Enable 1: Disable

7.2.5.15. TCON CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TCON_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: Bypass 1: Enable
30:0	/	/	/

7.2.5.16. TCON CEU Coefficient MUL Register (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)	Register Name: TCON_CEU_COEF_REG

Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

7.2.5.17. TCON CEU Coefficient Add Register (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: TCON_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_Coef_Add_Value Signed 19bit value, range of (-16384, 16384) N=0: Rc N=1: Gc N=2: Bc

7.2.5.18. TCON CEU Coefficient Range Register (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0,1,2)			Register Name: TCON_CEU_COEF_RANGE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255]

7.2.5.19. TCON Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TCON_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM

15:2	/	/	/
1:0	R/W	0x0	SAFE_PERIOD_MODE 00: Unsafe 01: Safe 10: Safe at ECC_FIFO_CUR_NUM > SAFE_PERIOD_FIFO_NUM 11: Safe at 2 and safe at sync active

7.2.5.20. TCON1 Fill Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TCON1_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON1_FILL_EN 0: Bypass 1: Enable
30:0	/	/	/

7.2.5.21. TCON1 Fill Begin Register (Default Value: 0x0000_0000)

Offset: 0x0304+N*0x0C(N=0,1,2)			Register Name: TCON1_FILL_BEGIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN

7.2.5.22. TCON1 Fill End Register (Default Value: 0x0000_0000)

Offset: 0x0308+N*0x0C(N=0,1,2)			Register Name: TCON1_FILL_END_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END

7.2.5.23. TCON1 Fill Data Register (Default Value: 0x0000_0000)

Offset: 0x030C+N*0x0C(N=0,1,2)			Register Name: TCON1_FILL_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_VALUE

7.2.6. TCON1 Module Register List

Module Name	Base Address
TCON1	0x01C0D000

Register Name	Offset	Description
TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON1_CTL_REG	0x0090	TCON1 Control Register
TCON1_BASIC0_REG	0x0094	TCON1 Basic Timing Register0
TCON1_BASIC1_REG	0x0098	TCON1 Basic Timing Register1
TCON1_BASIC2_REG	0x009C	TCON1 Basic Timing Register2
TCON1_BASIC3_REG	0x00A0	TCON1 Basic Timing Register3
TCON1_BASIC4_REG	0x00A4	TCON1 Basic Timing Register4
TCON1_BASIC5_REG	0x00A8	TCON1 Basic Timing Register5
TCON1_PS_SYNC_REG	0x00B0	TCON1 Sync Register
TCON1_IO_POL_REG	0x00F0	TCON1 IO Polarity Register
TCON1_IO_TRI_REG	0x00F4	TCON1 IO Trigger Register
TCON_ECC_FIFO_REG	0x00F8	TCON ECC FIFO Register
TCON_CEU_CTL_REG	0x0100	TCON CEU Control Register
TCON_CEU_COEF_MUL_REG	0x0110+N*0x04	TCON CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
TCON_CEU_COEF_ADD_REG	0x011C+N*0x10	TCON CEU Coefficient Register1(N=0,1,2)
TCON_CEU_COEF_RANG_REG	0x0140+N*0x04	TCON CEU Coefficient Register2(N=0,1,2)
TCON_SAFE_PERIOD_REG	0x01F0	TCON Safe Period Register
TCON1_FILL_CTL_REG	0x0300	TCON1 Fill Data Control Register
TCON1_FILL_BEGIN_REG	0x0304+N*0x0C	TCON1 Fill Data Begin Register(N=0,1,2)
TCON1_FILL_END_REG	0x0308+N*0x0C	TCON1 Fill Data End Register(N=0,1,2)
TCON1_FILL_DATA0_REG	0x030C+N*0x0C	TCON1 Fill Data Value Register(N=0,1,2)
TCON1_GAMMA_TABLE_REG	0x0400-0x07FF	
TCON_ECC_FIFO_BIST_REG	0x0FFC	

7.2.7. TCON1 Module Register Description

7.2.7.1. TCON Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TCON_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON_EN 0: Disable 1: Enable

			When it's disabled, the module will be reset to idle state.
30	R/W	0x0	TCON_GAMMA_EN 0: Disable 1: Enable
29:0	/	/	/

7.2.7.2. TCON Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: TCON_GINT0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TCON1_VB_INT_EN 0: Disable 1: Enable
29	/	/	/
28	R/W	0x0	TCON1_LINE_INT_EN 0: Disable 1: Enable
27:15	/	/	/
14	R/W	0x0	TCON1_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TCON1_LINE_INT_FLAG Trigger when SY1 match the current TCON1 scan line. Write 0 to clear it.
11:0	/	/	/

7.2.7.3. TCON Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: TCON_GINT1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	TCON1_LINE_INT_NUM Scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. **Note:** SY1 is writable only when LINE_TRG1 disable.

7.2.7.4. TCON1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TCON1_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON1_EN 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0x0	START_DELAY This is for DE1 and DE2
3:2	/	/	/
1	R/W	0x0	TCON1_SRC_SEL 0: Reserved 1: BLUE data(FIFO2 disable,RGB = 0000FF)
0	/	/	/

7.2.7.5. TCON1 Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: TCON1_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON1_XI Source width is X+1
15:12	/	/	/
11:0	R/W	0x0	TCON1_YI Source height is Y+1

7.2.7.6. TCON1 Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TCON1_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO Width is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO Width is LS_YO+1 **Note:** This version LS_YO = TCON1_YI

7.2.7.7. TCON1 Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TCON1_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON1_XO Width is TCON1_XO+1
15:12	/	/	/
11:0	R/W	0x0	TCON1_YO Height is TCON1_YO+1

7.2.7.8. TCON1 Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TCON1_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch Thbp = (HBP +1) * Thdclk

7.2.7.9. TCON1 Basic Timing Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TCON1_BASIC4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT Horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0x0	VBP Horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

7.2.7.10. TCON1 Basic Timing Register5 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TCON1_BASIC5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

25:16	R/W	0x0	HSPW Horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk **Note:** HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th **Note:** VT/2 > (VSPW+1)

7.2.7.11. TCON1 SYNC Register (Default Value: 0x0000_0000)

Offset: 0x00B0			**Register Name: TCON1_PS_SYNC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SYNC_X
15:0	R/W	0x0	SYNC_Y

7.2.7.12. TCON1 IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x00F0			**Register Name: TCON1_IO_POL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert
23:0	R/W	0x0	DATA_INV TCON output port D[23:0] polarity control,with independent bit control 0s: Normal polarity 1s: Invert the specify output

7.2.7.13. TCON1 IO Trigger Register (Default Value: 0x0FFF_FFFF)

Offset: 0x00F4			Register Name: TCON1_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 0: Enable 1: Disable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 0: Enable 1: Disable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 0: Enable 1: Disable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 0: Enable 1: Disable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN TCON output port D[23:0] output enable,with independent bit control. 0s: Enable 1s: Disable

7.2.7.14. TCON ECC FIFO Register (Default Value: UDF)

Offset: 0x00F8			Register Name: TCON_ECC_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	UDF	ECC_FIFO_BIST_EN 0: Disable 1: Enable
30	R/W	UDF	ECC_FIFO_ERR_FLAG
29:24	/	/	/
23:16	R/W	UDF	ECC_FIFO_ERR_BITS
15:9	/	/	/
8	R/W	UDF	ECC_FIFO_BLANK_EN 0: Disable ECC function in blanking

			1: Enable ECC function in blanking ECC function is tent to trigger in blanking area at hv mode, set '0' when in hv mode.
7:0	R/W	UDF	ECC_FIFO_SETTING Bit3 0: Enable 1: Disable

7.2.7.15. TCON CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			**Register Name: TCON_CEU_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: Bypass 1: Enable
30:0	/	/	/

7.2.7.16. TCON CEU Coefficient MUL Register (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			**Register Name: TCON_CEU_COEF_MUL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

7.2.7.17. TCON CEU Coefficient Add Register (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0,1,2)	**Register Name: TCON_CEU_COEF_ADD_REG**

Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19bit value, range of (-16384, 16384) N=0: Rc N=1: Gc N=2: Bc

7.2.7.18. TCON CEU Coefficient Rang Register (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0,1,2)			Register Name: TCON_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255]

7.2.7.19. TCON Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TCON_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM
15:2	/	/	/
1:0	R/W	0x0	SAFE_PERIOD_MODE 00: Unsafe 01: Safe 10: Safe at ECC_FIFO_CUR_NUM > SAFE_PERIOD_FIFO_NUM 11: Safe at 2 and safe at sync active

7.2.7.20. TCON1 Fill Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TCON1_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON1_FILL_EN 0: Bypass 1: Enable
30:0	/	/	/

7.2.7.21. TCON1 Fill Begin Register (Default Value: 0x0000_0000)

Offset: 0x0304+N*0x0C(N=0,1,2)			Register Name: TCON1_FILL_BEGIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN

7.2.7.22. TCON1 Fill End Register (Default Value: 0x0000_0000)

Offset: 0x0308+N*0x0C(N=0,1,2)			Register Name: TCON1_FILL_END_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END

7.2.7.23. TCON1 Fill Data Register (Default Value: 0x0000_0000)

Offset: 0x030C+N*0x0C(N=0,1,2)			Register Name: TCON1_FILL_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_VALUE

Chapter 8 Audio

This chapter describes the H5 audio, including:

- Audio Codec
- I2S/PCM
- OWA

8.1. Audio Codec

8.1.1. Overview

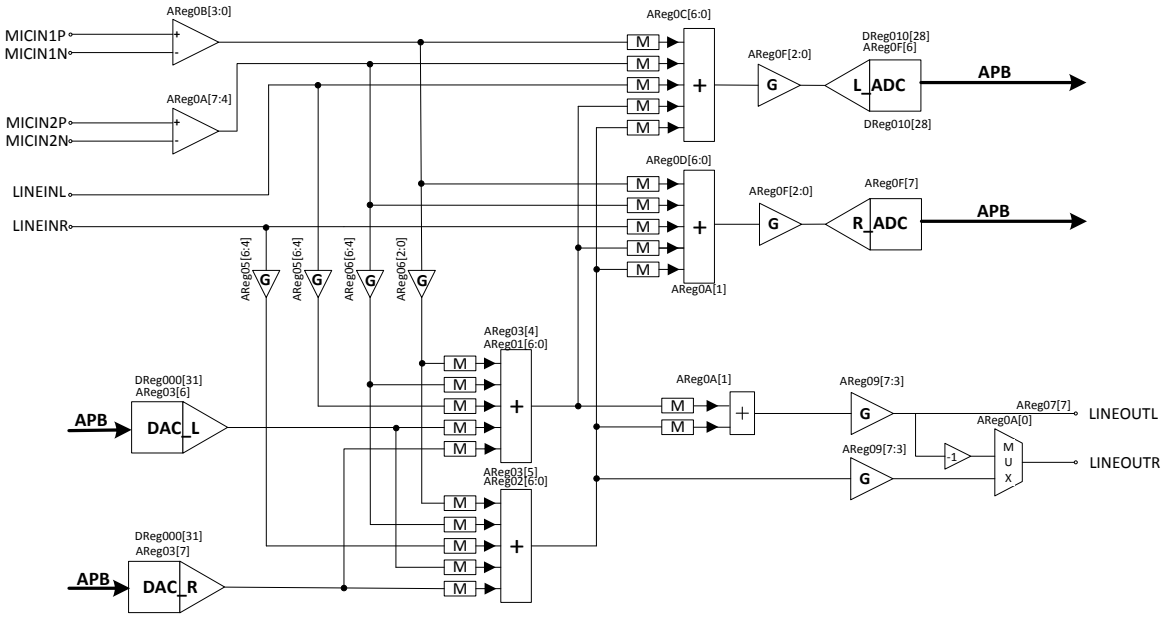
The embedded Audio Codec is a high-quality stereo audio codec designed for embed device. It provides a stereo DAC for playback, and a stereo ADC for recording.

Features:

- Two audio digital-to-analog(DAC) channels
  - 100±3dB SNR@A-weight
  - Supports DAC sample rate from 8KHz to 192KHz
- Two audio analog-to-digital(ADC) channels
  - 93±3dB SNR@A-weight
  - Supports ADC sample rate from 8KHz to 48KHz
- Supports analog/digital volume control
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- Supports Dynamic Range Control(DRC) adjusting the ADC recording output
- Three audio inputs:
  - Two differential microphone inputs
  - Stereo line-in L/R channel input
- One audio output:
  - Stereo line-out L/R channel output
- Interrupt and DMA support

8.1.2. Block Diagram

Figure 8-1 shows the block diagram of the Audio Codec.



Areg: Analog Register， Dreg: Digital Register

Figure 8-1. Audio Codec Block Diagram

8.1.3. Operations and Functional Descriptions

8.1.3.1. External Signals

The following table describes the external signals of Audio Codec.

Table 8-1. Audio Codec External Signals

Signal Name	Type	Description
Analog I/O Pins		
MICIN1P	AI	First microphone positive input
MICIN1N	AI	First microphone negative input
MICIN2P	AI	Second microphone positive input
MICIN2N	AI	Second microphone negative input
LINEINL	AI	Line in left channel input
LINEINR	AI	Line in right channel input
LINEOUTL	AO	Line out left channel output
LINEOUTR	AO	Line out right channel output
Filter/Reference		

MBIAS	AO	Bias voltage output for main microphone
VRA1	AO	Internal reference voltage
VRA2	AO	Internal reference voltage
VRP	AO	Internal reference voltage
Power/Ground		
AVCC	P	Analog power
AGND	G	Analog ground

8.1.3.2. Clock Sources

Figure 8-2 describes the clock sources for Audio Codec. Users can see **Chapter 4.3 CCU** for clock setting, configuration and gating information.

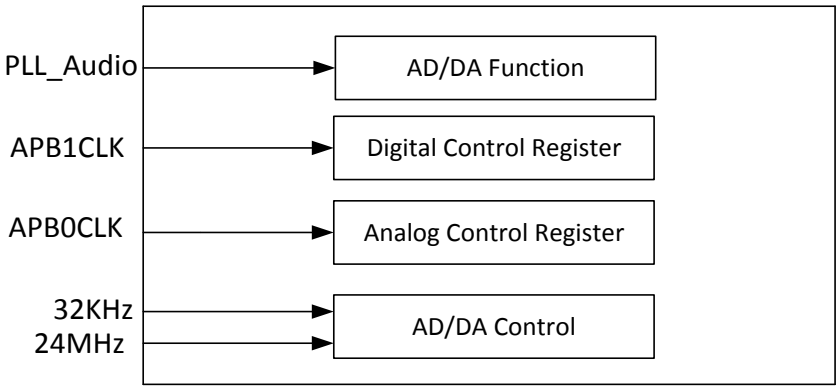


Figure 8-2. Audio Codec Clock Sources

8.1.3.3. Reset System

Figure 8-3 describes the Audio Codec analog part reset system, and Figure 8-4 describes the Audio Codec digital part reset system.

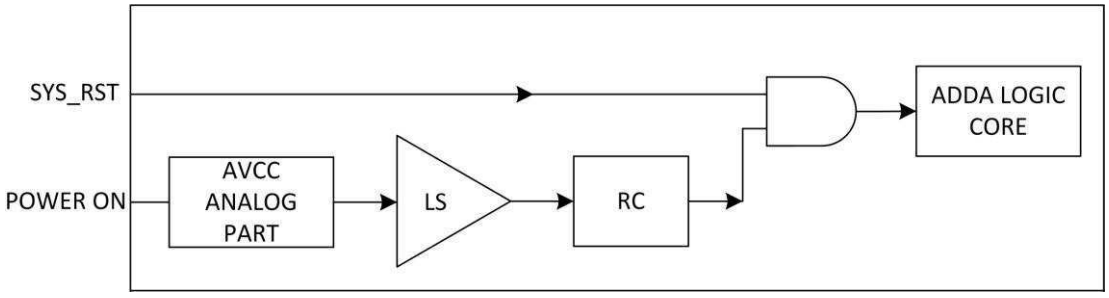


Figure 8-3. Audio Codec Analog Reset System

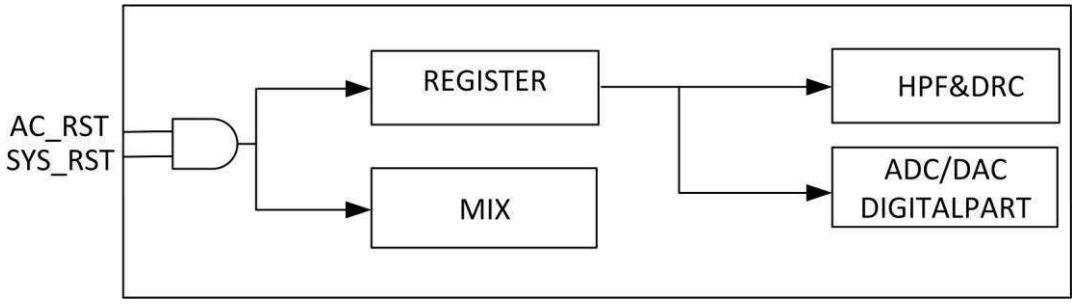


Figure 8-4. Audio Codec Digital Reset System

8.1.3.4. Power Domain

Audio Codec system needs three powers, AVCC、VDD-SYS and VDD-CPUS, is shown in Figure 8-5. The AVCC provides power for ADC/DAC and other analog part. VDD-SYS provides power for ADC/DAC digital control register, digital part and audio codec register. VDD-CPUS provides power for ADC/DAC analog control register .

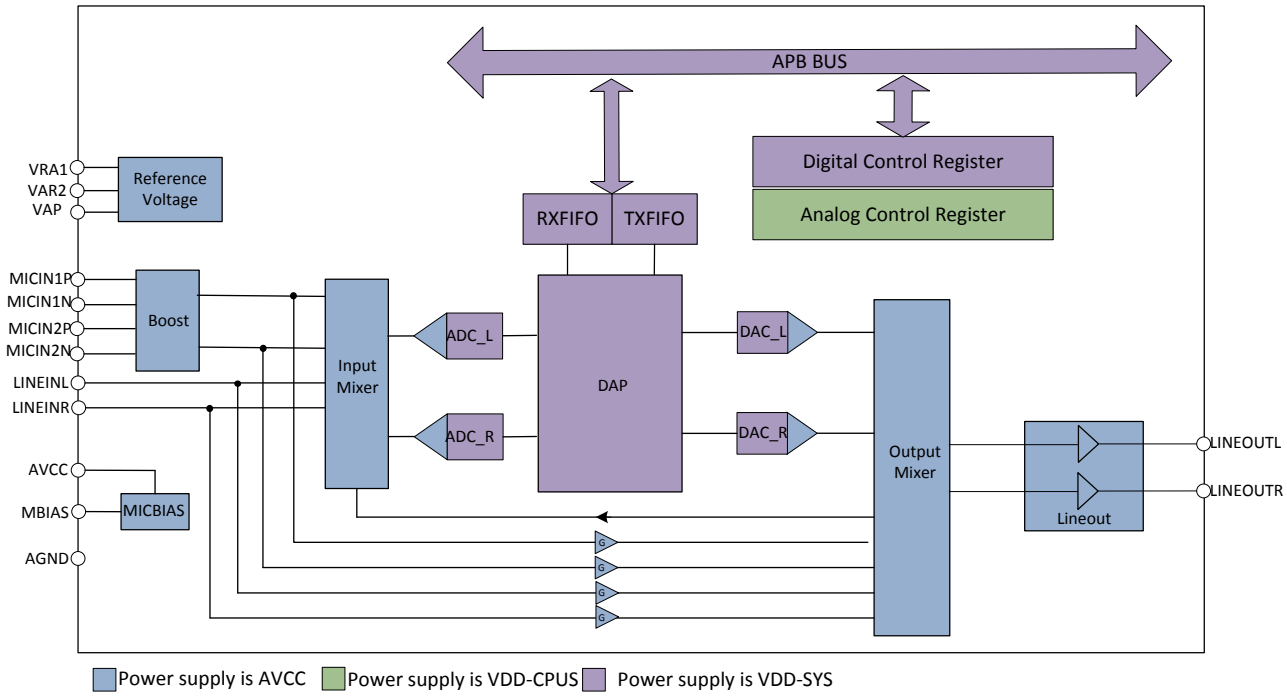


Figure 8-5. Audio Codec Power Domain

All power supplies are turned on in normal application, such as music play, record.

AVCC and VDD-CPUS are turned on in super standby mode and AA path mode.

All power supplies are closed in shutdown.

8.1.4. Register List

Module Name	Base Address
Audio Codec	0x01C22C00

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
AC_DAC_FIFOC	0x0004	DAC FIFO Control Register
AC_DAC_FIFOS	0x0008	DAC FIFO Status Register
/	0x000C	Reserved
AC_ADC_FIFOC	0x0010	ADC FIFO Control Register
AC_ADC_FIFOS	0x0014	ADC FIFO Status Register
AC_ADC_RXDATA	0x0018	ADC RX Data Register
AC_DAC_TXDATA	0x0020	DAC TX Data Register
/	0x0024~0x003C	Reserved
AC_DAC_CNT	0x0040	DAC TX FIFO Counter Register
AC_ADC_CNT	0x0044	ADC RX FIFO Counter Register
AC_DAC_DG	0x0048	DAC Debug Register
AC_ADC_DG	0x004C	ADC Debug Register
/	0x0050~0x005C	Reserved
AC_DAC_DAP_CTR	0x0060	DAC DAP Control Register
/	0x0064~0x006C	Reserved
AC_ADC_DAP_CTR	0x0070	ADC DAP Control Register
AC_ADC_DAP_LCTR	0x0074	ADC DAP Left Control Register
AC_ADC_DAP_RCTR	0x0078	ADC DAP Right Control Register
AC_ADC_DAP_PARA	0x007C	ADC DAP Parameter Register
AC_ADC_DAP_LAC	0x0080	ADC DAP Left Average Coef Register
AC_ADC_DAP_LDAT	0x0084	ADC DAP Left Decay and Attack Time Register
AC_ADC_DAP_RAC	0x0088	ADC DAP Right Average Coef Register
AC_ADC_DAP_RDAT	0x008C	ADC DAP Right Decay and Attack Time Register
AC_ADC_DAP_HPFC	0x0090	ADC DAP HPF Coef Register
AC_ADC_DAP_LINAC	0x0094	ADC DAP Left Input Signal Low Average Coef Register
AC_ADC_DAP_RINAC	0x0098	ADC DAP Right Input Signal Low Average Coef Register
AC_ADC_DAP_ORT	0x009C	ADC DAP Optimum Register
/	0x00A0~0x00FC	Reserved
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register

AC_DAC_DRC_RPFHRT	0x0124	DAC DRC Right Peak filter High Release Time Coef Register
AC_DAC_DRC_RPFLRT	0x0128	DAC DRC Right Peak filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_RRMSHAT	0x0134	DAC DRC Right RMS Filter High Coef Register
AC_DAC_DRC_RRMSLAT	0x0138	DAC DRC Right RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Theshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Theshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Theshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold
AC_DAC_DRC_HET	0x016C	DAC DRC Expander Theshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Theshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth Filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth Filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth Filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
/	0x01C0~0x01FC	Reserved
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register

AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_RPFHAT	0x0214	ADC DRC Right Peak Filter High Attack Time Coef Register
AC_ADC_DRC_RPFLAT	0x0218	ADC DRC Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_RPFHRT	0x0224	ADC DRC Right Peak filter High Release Time Coef Register
AC_ADC_DRC_RPFLRT	0x0228	ADC DRC Right Peak filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_RRMSHAT	0x0234	ADC DRC Right RMS Filter High Coef Register
AC_ADC_DRC_RRMSLAT	0x0238	ADC DRC Right RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Theshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Theshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Theshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Theshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Theshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGLS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register

AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
Analog Domain Register		
AC_PR_CFG		AC Parameter Configuration Register(0x01F015C0)
LINEOUT_PA_GAT	0x00	LINEOUT PA Gating Control Register
LOMIXSC	0x01	Left Output Mixer Source Select Control Register
ROMIXSC	0x02	Right Output Mixer Source Select Control Register
DAC_PA_SCR	0x03	DAC Analog Enable And PA Source Control Register
LINEIN_GCTR	0x05	Linein Gain Control Register
MIC_GCTR	0x06	MIC1 And MIC2 Gain Control Register
PAEN_CTR	0x07	PA Enable And LINEOUT Control Register
LINEOUT_VOLC	0x09	LINEOUT Volume Control Register
MIC2G_LINEOUT_CTR	0x0A	MIC2 Boost And LINEOUT Enable Control Register
MIC1G_MICBAIS_CTR	0x0B	MIC1 Boost And MICBIAS Control Register
LADCMIXSC	0x0C	Left ADC Mixer Source Control Register
RADCMIXSC	0x0D	Right Mixer Source Control Register
RES_REG	0x0E	Reserved Register
ADC_AP_EN	0x0F	ADC Analog Part Enable Register
ADDA_APT0	0x10	ADDA Analog Performance Turning0 Register
ADDA_APT1	0x11	ADDA Analog Performance Turning1 Register
ADDA_APT2	0x12	ADDA Analog Performance Turning2 Register
BIAS_DA16_CTR0	0x13	Bias & DA16 Calibration Control Register0
BIAS_DA16_CTR1	0x14	Bias & DA16 Calibration Control Register1
DA16CAL	0x15	DA16 Calibration Data Register
DA16VERIFY	0x16	DA16 Register Setting Data Register
BIASCALI	0x17	BIAS Calibration Data Register
BIASVERIFY	0x18	BIAS Register Setting Data Register

8.1.5. Register Description

8.1.5.1. 0x00 DAC Digital Part Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: AC_DAC_DPC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EN_DAC DAC Digital Part Enable 0: Disable 1 : Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels

			Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT=DVC[5:0]*(-1.16Db) 64 steps, -1.16Db/step
11:1	/	/	/
0	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable

8.1.5.2. 0x04 DAC FIFO Control Register (Default Value: 0x0000_4000)

Offset: 0x0004			**Register Name: AC_DAC_FIFOC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	DAC_FS Sample Rate Of DAC 000: 48KHz 010: 24KHz 100: 12KHz 110: 192KHz 001: 32KHz 011: 16KHz 101: 8KHz 111: 96KHz 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO underrun

			0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 24-bit transmitted audio sample: 00,10: FIFO_I[23:0] = {TXDATA[31:8]} 01,11: Reserved For 16-bit transmitted audio sample: 00,10: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 01,11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO Available Room is less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: IRQ/DRQ de-asserted When WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ generated when WLEVEL ≤ TXTL **Note:** (1). WLEVEL represents the number of valid samples in the TX FIFO (2). Only TXTL[6:0] valid when TXMODE = 0
7	R/W	0x0	ADDA_LOOP_EN ADDA Loop Enable 0: Disable 1: Enable
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 Levels FIFO 1: Mono, 128 Levels FIFO When Enabled, L & R Channel Send Same Data
5	R/W	0x0	TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN

			DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Underrun IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W1C	0x0	FIFO_FLUSH DAC FIFO Flush Write '1' to flush TX FIFO, Self clear to '0'

8.1.5.3. 0x08 DAC FIFO Status Register(Default Value: 0x0080_0088)

Offset: 0x0008			Register Name: AC_DAC_FIFOS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatically clear if interrupt condition fails

2	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

8.1.5.4. 0x10 ADC FIFO Control Register(Default Value: 0x0000_0F00)

Offset: 0x0010			**Register Name: AC_ADC_FIFOC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz 011: 16KHz 101: 8KHz 111: Reserved 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register

			For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:19	/	/	/
18:17	R/W	0x0	ADCFDT ADC FIFO Delay Time for Writing Data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms
16	R/W	0x0	ADCDFEN ADC FIFO Delay Function for Writing Data after EN_AD 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0xF	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ generated when WLEVEL < RXTL[4:0] WLEVEL represents the number of valid samples in the RX FIFO.
7	R/W	0x0	ADC_MONO_EN ADC Mono Enable 0: Stereo, 16 levels FIFO 1: Mono, 32 levels FIFO When it is set to '1', Only left channel samples are recorded
6	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits
5	/	/	/
4	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable

			1: Enable
3	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
2	/	/	
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

8.1.5.5. 0x14 ADC FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: AC_ADC_FIFOS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:14	/	/	/
13:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W1C	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails
2	/	/	/
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ

			Write '1' to clear this interrupt
0	/	/	/

8.1.5.6. 0x18 ADC RX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

8.1.5.7. 0x20 DAC TX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

8.1.5.8. 0x40 DAC TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_DAC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value **Note:** It is used for Audio/ Video Synchronization.

8.1.5.9. 0x44 ADC RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter

			The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value. **Note:** It is used for Audio/ Video Synchronization.

8.1.5.10. 0x48 DAC Debug Register (Default Value: 0x0000_0000)

Offset: 0x0048			**Register Name: AC_DAC_DG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT. DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: Silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC Clock from PLL 1: CODEC Clock from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC Output Channel Swap Enable 0:Disable 1:Enable
5:0	/	/	/

8.1.5.11. 0x4C ADC Debug Register (Default Value: 0x0000_0000)

Offset: 0x004C			**Register Name: AC_ADC_DG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	AD_SWP

			ADC Output Channel Swap Enable (for digital filter) 0: Disable 1: Enable
23:0	/	/	/

8.1.5.12. 0x60 DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: AC_DAC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDAP _EN DAP for DAC Enable 0: Bypass 1: Enable
30:16	/	/	/
15	R/W	0x0	DAC_DRC_EN DRC Enable Control 0: Disable 1: Enable
14	R/W	0x0	DAC_DRC_HPF_EN HPF Enable Control 0: Disable 1: Enable
13:0	/	/	/

8.1.5.13. 0x70 ADC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: AC_ADC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADAP _EN DAP for ADC Enable 0: Bypass 1: Enable
30	R/W	0x0	ADAP_START. DAP for ADC Start up 0: Disable 1: Start up
29:27	/	/	/

26	R/W	0x0	ENADC_DRC DRC for ADC Enable 0: Bypass 1: Enable
25	R/W	0x0	ADC_DRC_EN ADC DRC Function Enable
24	R/W	0x0	ADC_DRC_HPF_EN ADC DRC HPF Function Enable
23:22	/	/	/
21	R	0x0	ADAP_LSATU_FLAG. Left Channel AGC Saturation Flag 0: No saturation 1: Saturation
20	R	0x0	ADAP_LNOI_FLAG. Left Channel AGC Noise-Threshold Flag 0: No noise-threshold 1: Noise-threshold
19:12	R	0x0	ADAP_LCHAN_GAIN Left Channel Gain Applied by AGC (7.1format 2s component(-20dB – 40dB), 0.5dB/ step) 0x50 : 40dB 0x4F : 39.5dB ---------- 0x00 : 00dB 0xFF : -0.5dB
11:10	/	/	/
9	R	0x0	ADAP_RSATU_FLAG. Right AGC Saturation Flag 0: No saturation 1: Saturation
8	R	0x0	ADAP_RNOI_FLAG. Right Channel AGC Noise-Threshold Flag 0: No noise-threshold 1: Noise-threshold
7:0	R	0x0	ADAP_LCHAN_GAIN. Right Channel Gain Applied by AGC (7.1format 2s component)(0.5dB step) 0x50 : 40dB 0x4F : 39.5dB

			---------- 0x00 : 00dB 0xFF : -0.5dB

8.1.5.14. 0x74 ADC DAP Left Control Register (Default Value: 0x001F_7000)

Offset: 0x0074			Register Name: AC_ADC_DAP_LCTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x1F	ADAP_LNOI_SET. Left Channel Noise Threshold Setting 0x00 : -24dB 0x01 : -26dB 0x02 : -28dB ---------- 0x1D: -82dB 0x1E: -84dB 0x1F: -86dB
15	/	/	/
14	R/W	0x1	AAGC_LCHAN_EN. Left AGC Function Enable 0: Disable 1: Enable
13	R/W	0x1	ADAP_LHPF_EN. Left HPF Enable 0: Disable 1: Enable
12	R/W	0x1	ADAP_RNOI_DET. Left Noise Detect Enable 0: Disable 1:Enable
11:10	/	/	/
9:8	R/W	0x0	ADAP_LCHAN_HYS. Left Hysteresis Setting 00 : 1dB 01 : 2dB 10 : 4dB 11 : Disable
7:4	R/W	0x0	ADAP_LNOI_DEB.

			Left Noise Debounce Time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111 :16*4096/fs $T=2^{(N+1)}$/fs ,except N=0
3:0	R/W	0x0	ADAP_LSIG_DEB. Left Signal Debounce Time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111 :16*4096/fs $T=2^{(N+1)}$/fs ,except N=0

8.1.5.15. 0x78 ADC DAP Right Control Register (Default Value: 0x001F_7000)

Offset: 0x0078			**Register Name: AC_ADC_DAP_RCTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x1F	ADAP_RNOI_SET. Right Channel Noise Threshold Setting 0x00 : -24dB 0x01 : -26dB 0x02 : -28dB ---------- 0x1D: -82dB 0x1E: -84dB 0x1F: -86dB
15	/	/	/
14	R/W	0x1	AAGC_RCHAN_EN. Right AGC Enable 0: Disable 1: Enable
13	R/W	0x1	ADAP_RHPF_EN. Right HPF Enable

			0: Disable 1: Enable
12	R/W	0x1	ADAP_RNOI_DET. Right Noise Detect Enable 0: Disable 1: Enable
11:10	/	/	/
9:8	R/W	0x0	ADAP_RCHAN_HYS. Right Hysteresis Setting 00: 1dB 01: 2dB 10: 4dB 11: Disable
7:4	R/W	0x0	ADAP_RNOI_DEB. Right Noise Debounce Time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111：16*4096/fs $T=2^{(N+1)}/fs$,except N=0
3:0	R/W	0x0	ADAP_RSIG_DEB. Right Signal Debounce Time 0000:0/fs 0001:4/fs 0010:8/fs ---------- 1111：16*4096/fs $T=2^{(N+1)}/fs$,except N=0

8.1.5.16. 0x7C ADC DAP Parameter Register (Default Value: 0x2C2C_2828)

Offset: 0x007C			**Register Name: AC_ADC_DAP_PARA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x2C	ADAP_LTARG_SET. Left Channel Target Level Setting (-1dB ~ -30dB). (6.0format 2s component)
23:22	/	/	/

21:16	R/W	0x2C	ADAP_RTARG_SET. Right Channel Target Level Setting (-1dB ~ -30dB). (6.0format 2s component)
15:8	R/W	0x28	ADAP_LGAIN_MAX. Left Channel Max Gain Setting (0dB ~ 40dB). (7.1format 2s component)
7:0	R/W	0x28	ADAP_RGAIN_MAX. Right Channel Max Gain Setting (0dB ~ 40dB). (7.1format 2s component)

8.1.5.17. 0x80 ADC DAP Left Average Coef Register (Default Value: 0x0005_1EB8)

Offset: 0x0080			**Register Name: AC_ADC_DAP_LAC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_LAC. Average Level Coefficient Setting(3.24format 2s component)

8.1.5.18. 0x84 ADC DAP Left Decay & Attack Time Register (Default Value: 0x0000_001F)

Offset: 0x0084			**Register Name: AC_ADC_DAP_LDAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x0000	ADAP_LATT_SET Left Attack Time Coefficient Setting 000000000000000: 1x32/fs 000000000000001: 2x32/fs ---------- 111111111111111: 2^{15} x32/fs T=(n+1)*32*fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.
15	/	/	/
14:0	R/W	0x001F	ADAP_LDEC_SET Left Decay Time Coefficient Setting 000000000000000: 1x32/fs 000000000000001: 2x32/fs ---------- 000000000011111: 32x32/fs ---------- 111111111111111: 2^{15} x32/fs T=(n+1)*32/fs

			When the gain increases, the actual gain will increase 0.5dB at every decay time.

8.1.5.19. 0x88 ADC DAP Right Average Coef Register (Default Value: 0x0005_1EB8)

Offset: 0x0088			Register Name: AC_ADC_DAP_RAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_RAC. Average Level Coefficient Setting(3.24fomat)

8.1.5.20. 0x8C ADC DAP Right Decay & Attack Time Register (Default Value: 0x0000_001F)

Offset: 0x008C			Register Name: AC_ADC_DAP_RDAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x0000	ADAP_RATT_SET. Right Attack Time Coefficient Setting 000000000000000: 1x32/fs 000000000000001: 2x32/fs ---------- 111111111111111: 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.
15	/	/	/
14:0	R/W	0x001F	ADAP_RDEC_SET Right Decay Time Coefficient Setting 000000000000000: 1x32/fs 000000000000001: 2x32/fs ---------- 000000000011111: 32x32/fs ---------- 111111111111111: 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

8.1.5.21. 0x90 ADC DAP HPF Coef Register (Default Value: 0x00FF_FAC1)

Offset: 0x0090			Register Name: AC_ADC_DAP_HPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:0	R/W	0x0FFFAC1	ADAP_HPFC. HPF Coefficient Setting (3.24fomat)

8.1.5.22. 0x94 ADC DAP Left Input Signal Low Average Coef Register (Default Value: 0x0005_1EB8)

Offset: 0x0094			Register Name: AC_ADC_DAP_LINAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_LINAC Left input signal average filter coefficient to check noise or not (the coefficientis 3.24 format 2s complement) always the same as the left output signal average filter's.

8.1.5.23. 0x98 ADC DAP Right Input Signal Low Average Coef Register (Default Value: 0x0005_1EB8)

Offset: 0x0098			Register Name: AC_ADC_DAP_RNAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:0	R/W	0x0051EB8	ADAP_RINAC Right input signal average filter coefficient to check noise or not (the coefficientis 3.24 format 2s complement) always the same as the left output signal average filter's.

8.1.5.24. 0x9C ADC DAP Optimum Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: AC_ADC_DAP_OPT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	Left Energy Default Value Setting(include the input and output) 0: Min 1: Max
9:8	R/W	0x0	Left Channel Gain Hystersis Setting. The different between target level and the signal level must larger than the hystersis when the gain changed. 00: 0.4375dB

			01: 0.9375dB 10: 1.9375dB 11: 3dB
7:6	/	/	/
5	R/W	0x0	Input Signal Average Filter Coefficient Setting 0: The reg94/reg98 1: The reg80/reg88
4	R/W	0x0	AGC Output when the Channel in Noise State 0: Output is zero 1: Output is the input data
3	/	/	/
2	R/W	0x0	Right Energy Default Value Setting(include the input and output) 0 : Min 1 : Max
1:0	R/W	0x0	Right Channel Gain Hysteresis Setting. The different between target level and the signal level must larger than the hysteresis when the gain changed. 00 : 0.4375dB 01 : 0.9375dB 10 : 1.9375dB 11 : 3dB

8.1.5.25. 0x100 DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

8.1.5.26. 0x104 DAC DRC Low HPF Coef Register(Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

8.1.5.27. 0x108 DAC DRC Control Register(Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when DRC delay function is enabled and the DRC funciton is disabled. After disable DRC function and this bit is set to 0, the user should write the DRC delay function bit to 0. 0 : Not complete 1 : Complete
14:10	/	/	/
13:8	R/W	0x0	Signal Delay Time Setting 000000 : (8x1)fs 000001 : (8x2)fs 000010 : (8x3)fs ---------- 101110 : (8*47)fs 101111 : (8*48)fs 110000 ~ 111111 : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30. When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the DRC disable and the drc buffer data output completely. 0 : Don't use the buffer 1 : Use the buffer
6	R/W	0x0	DRC Gain Max Limit Enable 0 : Disable 1 : Enable
5	R/W	0x0	DRC Gain Min Limit Enable. When this function enable, it will overwrite the noise detect function. 0 : Disable 1 : Enable
4	R/W	0x0	Control DRC to Detect Noise when ET Enable 0 : Disable 1 : Enable
3	R/W	0x0	Signal Function Select 0 : RMS filter

			1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay Function Enable 0 : Disable 1 : Enable When the **Delay function enable** bit is disabled, the Signal delay time is unused.
1	R/W	0x0	DRC LT Enable 0 : Disable 1 : Enable When the **DRC LT enable** bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET Enable 0 : Disable 1 : Enable When the **DRC ET enable** bit is disabled, Ke and OPE parameter is unused.

8.1.5.28. 0x10C DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			**Register Name: AC_DAC_DRC_LPFHAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.29. 0x110 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			**Register Name: AC_DAC_DRC_LPFLAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.30. 0x114 DAC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0114			Register Name: AC_DAC_DRC_RPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.31. 0x118 DAC DRC Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.32. 0x11C DAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.33. 0x120 DAC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.34. 0x124 DAC DRC Right Peak filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0124			Register Name: AC_DAC_DRC_RPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter attack time parameter setting, which is determined by the

			equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.35. 0x128 DAC DRC Right Peak filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0128			Register Name: AC_DAC_DRC_RPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.36. 0x12C DAC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.37. 0x130 DAC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.38. 0x134 DAC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0134			Register Name: AC_DAC_DRC_RRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0001	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.39. 0x138 DAC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0138			Register Name: AC_DAC_DRC_RRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.40. 0x13C DAC DRC Compressor Threshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

8.1.5.41. 0x140 DAC DRC Compressor Threshold Low Setting Register (Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

8.1.5.42. 0x144 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor is determined by the equation that Kc = 1/R, R is the ratio of the compressor, which always is interger. The format is 6.24. (2 : 1)

8.1.5.43. 0x148 DAC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor is determined by the equation that Kc = 1/R, R is the ratio of the compressor, which always is interger. The format is 6.24. (2 : 1)

8.1.5.44. 0x14C DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor is determined by the equation -OPC/6.0206. The format is 8.24 (-40dB)

8.1.5.45. 0x150 DAC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor is determined by the equation OPC/6.0206. The format is 8.24 (-40dB)

8.1.5.46. 0x154 DAC DRC Limiter Theshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting is set by the equation that LTin = -LT/6.0206. The format is 8.24. (-10dB)

8.1.5.47. 0x158 DAC DRC Limiter Theshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting is set by the equation that LTin = -LT/6.0206.The format is 8.24. (-10dB)

8.1.5.48. 0x15C DAC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter is determined by the equation that Kl = 1/R, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

8.1.5.49. 0x160 DAC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter is determined by the equation that Kl = 1/R, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

8.1.5.50. 0x164 DAC DRC Limiter High Output at Limiter Threshold (Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter is determined by equation OPT/6.0206. The format is 8.24 (-25dB)

8.1.5.51. 0x168 DAC DRC Limiter Low Output at Limiter Threshold (Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter is determined by equation OPT/6.0206. The format is 8.24 (-25dB)

8.1.5.52. 0x16C DAC DRC Expander Theshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting is set by the equation that ETin = -ET/6.0206. The format is 8.24. (-70dB)

8.1.5.53. 0x170 DAC DRC Expander Theshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting is set by the equation that ETin = -ET/6.0206. The format is 8.24. (-70dB)

8.1.5.54. 0x174 DAC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0500	The slope of the expander is determined by the equation that Ke = 1/R, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

8.1.5.55. 0x178 DAC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander is determined by the equation that Ke = 1/R, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

8.1.5.56. 0x17C DAC DRC Expander High Output at Expander Threshold (Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander is determined by equation OPE/6.0206. The format is 8.24 (-70dB)

8.1.5.57. 0x180 DAC DRC Expander Low Output at Expander Threshold (Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander is determined by equation OPE/6.0206. The format is 8.24 (-70dB)

8.1.5.58. 0x184 DAC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/

13:0	R/W	0x0100	The slope of the linear is determined by the equation that Kn = 1/R, R is the ratio of the linear, which always is interger . The format is 6.24. (1:1)

8.1.5.59. 0x188 DAC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear is determined by the equation that Kn = 1/R, R is the ratio of the linear, which always is interger . The format is 6.24. (1:1)

8.1.5.60. 0x18C DAC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting,which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

8.1.5.61. 0x190 DAC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting,which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

8.1.5.62. 0x194 DAC DRC Smooth filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

8.1.5.63. 0x198 DAC DRC Smooth filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0198	Register Name: AC_DAC_DRC_SFLRT

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

8.1.5.64. 0x19C DAC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFE56	The maximum gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

8.1.5.65. 0x1A0 DAC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	The maximum gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

8.1.5.66. 0x1A4 DAC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	The minimum gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤-30dB (-40dB)

8.1.5.67. 0x1A8 DAC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The minimum gain setting is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤-30dB (-40dB)

8.1.5.68. 0x1AC DAC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x01AC	Register Name: AC_DAC_DRC_EPSHC

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	/	/	/
11:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

8.1.5.69. 0x1B0 DAC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

8.1.5.70. 0x1B8 DAC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0100	The gain of the HPF high coefficient setting . The format is 3.24.(gain = 1)

8.1.5.71. 0x1BC DAC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the HPF low coefficient setting. The format is 3.24.(gain = 1)

8.1.5.72. 0x200 ADC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

8.1.5.73. 0x204 ADC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

8.1.5.74. 0x208 ADC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when DRC delay function is enabled and the DRC function is disabled. After disabled DRC function and this bit changed to 0, the user should write the DRC delay function bit to 0. 0 : Not complete 1 : Complete
14:10	/	/	/
13:8	R/W	0x0	Signal Delay Time Setting 000000 : (8x1)fs 000001 : (8x2)fs 000010 : (8x3)fs ---------- 101110 : (8*47)fs 101111 : (8*48)fs 110000 ~ 111111 : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the DRC disable and the DRC buffer data output completely. 0 : Don't use the buffer 1 : Use the buffer
6	R/W	0x0	DRC Gain Max Limit Enable 0 : Disable 1 : Enable
5	R/W	0x0	DRC Gain Min Limit Enable. When this function enable, it will overwrite the noise detect function.

			0 : Disable 1 : Enable
4	R/W	0x0	Control the DRC to Detect Noise when ET Enable 0 : Disable 1 : Enable
3	R/W	0x0	Signal Function Select 0 : RMS filter 1 : Peak filter When Signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When Signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/ AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay Function Enable 0 : Disable 1 : Enable When the Delay function is disabled, the Signal delay time is unused.
1	R/W	0x0	DRC LT Enable 0 : Disable 1 : Enable When the DRC LT disables the LT, then Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET Enable 0 : Disable 1 : Enable When the DRC ET disables the ET, then Ke and OPE parameter is unused.

8.1.5.75. 0x20C ADC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.76. 0x210 ADC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.77. 0x214 ADC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0214			Register Name: AC_ADC_DRC_RPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.78. 0x218 ADC DRC Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0218			Register Name: AC_ADC_DRC_RPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

8.1.5.79. 0x21C ADC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.80. 0x220 ADC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.81. 0x224 ADC DRC Right Peak filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0224			Register Name: AC_ADC_DRC_RPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter attack time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.82. 0x228 ADC DRC Right Peak filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

8.1.5.83. 0x22C ADC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.84. 0x230 ADC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.85. 0x234 ADC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0234			Register Name: AC_ADC_DRC_RRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:11	/	/	/
10:0	R/W	0x0001	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.86. 0x238 ADC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0238			Register Name: AC_ADC_DRC_RRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

8.1.5.87. 0x23C ADC DRC Compressor Theshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

8.1.5.88. 0x240 ADC DRC Compressor Theshold Low Setting Register (Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

8.1.5.89. 0x244 ADC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor is determined by the equation that Kc = 1/R, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

8.1.5.90. 0x248 ADC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0248	Register Name: AC_ADC_DRC_LKC

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor is determined by the equation that Kc = 1/R, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

8.1.5.91. 0x24C ADC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor is determined by the equation OPC/6.0206. The format is 8.24. (-40dB)

8.1.5.92. 0x250 ADC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor is determined by the equation OPC/6.0206. The format is 8.24. (-40dB)

8.1.5.93. 0x254 ADC DRC Limiter Theshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting is set by the equation that LTin = -LT/6.0206. The format is 8.24. (-10dB)

8.1.5.94. 0x258 ADC DRC Limiter Theshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting is set by the equation that LTin = -LT/6.0206. The format is 8.24. (-10dB)

8.1.5.95. 0x25C ADC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x025C	Register Name: AC_ADC_DRC_HKl

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter is determined by the equation that Kl = 1/R, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

8.1.5.96. 0x260 ADC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter is determined by the equation that Kl = 1/R, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

8.1.5.97. 0x264 ADC DRC Limiter High Output at Limiter Threshold Register (Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter is determined by equation OPT/6.0206. The format is 8.24. (-25dB)

8.1.5.98. 0x268 ADC DRC Limiter Low Output at Limiter Threshold Register (Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter is determined by equation OPT/6.0206. The format is 8.24. (-25dB)

8.1.5.99. 0x26C ADC DRC Expander Theshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting is set by the equation that ETin = -ET/6.0206. The format is 8.24. (-70dB)

8.1.5.100. 0x270 ADC DRC Expander Theshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting is set by the equation that ETin = -ET/6.0206. The format is 8.24. (-70dB)

8.1.5.101. 0x274 ADC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0500	The slope of the expander is determined by the equation that Ke = 1/R, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

8.1.5.102. 0x278 ADC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander is determined by the equation that Ke = 1/R, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

8.1.5.103. 0x27C ADC DRC Expander High Output at Expander Threshold (Default Value: 0x0000_F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander is determined by equation OPE/6.0206. The format is 8.24. (-70dB)

8.1.5.104. 0x280 ADC DRC Expander Low Output at Expander Threshold (Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander is determined by equation OPE/6.0206. The format

			is 8.24. (-70dB)

8.1.5.105. 0x284 ADC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0100	The slope of the linear is determined by the equation that Kn = 1/R, R is the ratio of the linear, which always is interger . The format is 6.24. (1:1)

8.1.5.106. 0x288 ADC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear is determined by the equation that Kn = 1/R, R is the ratio of the linear, which always is interger . The format is 6.24. (1:1)

8.1.5.107. 0x28C ADC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

8.1.5.108. 0x290 ADC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

8.1.5.109. 0x294 ADC DRC Smooth filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

8.1.5.110. 0x298 ADC DRC Smooth filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

8.1.5.111. 0x29C ADC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

8.1.5.112. 0x2A0 ADC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

8.1.5.113. 0x2A4 ADC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -30dB (-40dB)

8.1.5.114. 0x2A8 ADC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x02A8	Register Name: AC_ADC_DRC_MNGLS

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -30dB (-40dB)

8.1.5.115. 0x2AC ADC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Writte	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

8.1.5.116. 0x2B0 ADC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

8.1.5.117. 0x2B8 ADC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

8.1.5.118. 0x2BC ADC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

8.1.6. Analog Part Register Description

8.1.6.1. AC Parameter Configuration Register (Default Value: 0x1000_0000)

Address: 0x01F015C0			Register Name: AC_PR_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	AC_PR_RST AC_PR Reset 0: Assert 1: De-assert
27:25	/	/	/
24	R/W	0x0	AC_PR_RW AC_PR Read or Write 0: Read 1: Write
23:21	/	/	/
20:16	R/W	0x0	AC_PR _ADDR AC_PR Address [4:0]
15:8	R/W	0x0	ADDA_PR _WDAT ADDA_PR Write Data [7:0]
7:0	R/W	0x0	ADDA_PR _RDAT ADDA_PR Read Data [7:0]

Note: The address of this Register is 0x01F015C0, using this register to configure the AC_PR register.

Reset: Reset signal;

ADDR[4:0]: AC_PR Address;

W/R: Write/Read Enable;

WDAT[7:0]: Write Data;

RDAT[7:0]: Read Data.

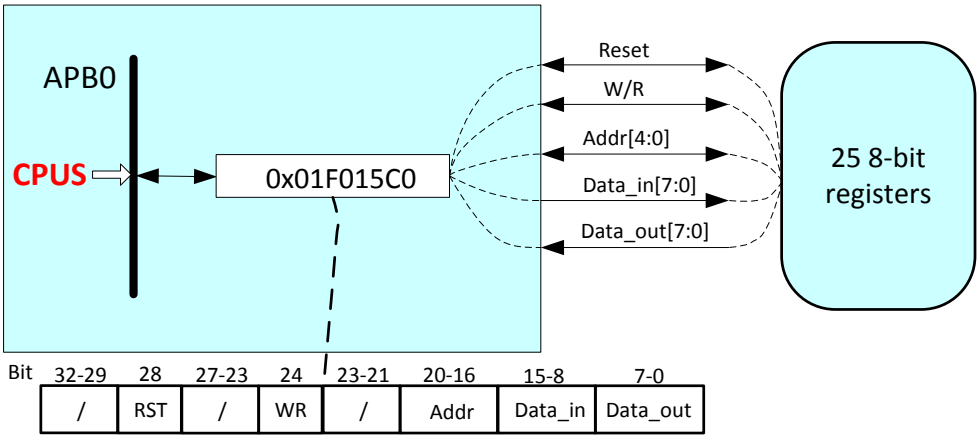


Figure 8-6. Audio Codec Analog Register Diagram

8.1.6.2. 0x00 LINEOUT PA Gating Control Register (Default Value: 0x00)

Offset:0x00			Register Name: LINEOUT_PA_GAT
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	PA clock gating control When system VDD is off and Audio analog channel is working.The bit must be set to 1, because the PA clock come from system VDD domain. When this bit is 1, the Zero cross over function will be disabled automatically. 0: Not gating 1: Gating
6:0	/	/	/

8.1.6.3. 0x01 Left Output Mixer Source Select Control Register (Default Value: 0x00)

Offset:0x01			Register Name: LOMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	LMIXMUTE Left Output Mixer Mute Control 0:Mute 1:Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: / Bit 3: / Bit 2: LINEINL Bit 1: Left Channel DAC Bit 0: Right Channel DAC

8.1.6.4. 0x02 Right Output Mixer Source Select Control Register (Default Value: 0x00)

Offset:0x02			Register Name: ROMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RMIXMUTE Right Output Mixer Mute Control 0: Mute

			1: Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: / Bit 3: / Bit 2: LINEINR Bit 1: Right Channel DAC Bit 0: Left Channel DAC

8.1.6.5. 0x03 DAC Analog Enable and PA Source Control Register (Default Value: 0x00)

Offset:0x03			**Register Name: DAC_PA_SRC**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	DACAREN Internal Analog Right Channel DAC Enable 0:Disable 1:Enable
6	R/W	0x0	DACALEN Internal Analog Left Channel DAC Enable 0:Disable 1:Enable
5	R/W	0x0	RMIXEN Right Analog Output Mixer Enable 0:Disable 1:Enable
4	R/W	0x0	LMIXEN Left Analog Output Mixer Enable 0:Disable 1:Enable
3:0	/	/	/

8.1.6.6. 0x05 Linein and Gain Control Register (Default Value: 0x30)

Offset:0x05			**Register Name: LINEIN_GCTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	LINEING LINEINL/R to L/R output mixer gain control

			From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3:0	/	/	/

8.1.6.7. 0x06 MIC1 And MIC2 Gain Control Register (Default Value: 0x33)

Offset:0x06			Register Name: MIC_GCTR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	MIC1_GAIN MIC1 BOOST stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x3	MIC2G, (volm2) MIC2 BOOST stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

8.1.6.8. 0x07 PA Enable and LINEOUT Control Register (Default Value: 0x04)

Offset:0x07			Register Name: PAEN_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	LINEOUTEN Right & Left LINEOUT Enable 0:Disable 1:Enable
6:4	/	/	/
3:2	R/W	0x1	PA_ANTI_POP_CTRL (slopelengthsel) PA Anti-Pop Time Control 00:131ms 01: 262ms 10: 393ms 11:524ms
1:0	/	/	/

8.1.6.9. 0x09 Lineout Volume Control Register (Default Value: 0x00)

Offset:0x09			Register Name: LINEOUT_VOLC
Bit	**Read/Write**	**Default/Hex**	**Description**
7:3	R/W	0x0	LINEOUTVOL Line-out Volume Control. Total 31 level, from 0dB to -48dB, 1.5dB/step, mute when 00000 & 00001

2:0	/	/	/

8.1.6.10. 0x0A Mic2 Boost and Lineout Enable Control Register (Default Value: 0x40)

Offset:0x0A			Register Name: MIC2G_LINEOUT_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0: Disable 1: Enable
6:4	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 000: 0dB 001~111: 24dB to 42dB(3dB/step) The default is 33dB
3	R/W	0x0	Line-out Left Select 0: Not select 1: Select
2	R/W	0x0	Line-out Right Select 0: Not select 1: Select
1	R/W	0x0	Left Line-out Source Select 0: Left output mixer 1: Left output mixer + right output mixer
0	R/W	0x0	Right Line-out Source Select 0: Right output mixer 1: Left line-out, for differential output

8.1.6.11. 0x0B MIC1 Boost and MICBIAS Control Register (Default Value: 0x04)

Offset:0x0B			Register Name: MIC1G_MICBAIS_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6	R/W	0x0	MMICBIASEN Master Microphone Bias Enable 0: Disable

			1: Enable
5:4	/	/	/
3	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0: Disable 1: Enable
2:0	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 000: 0dB 001~111: 24dB to 42dB(3dB/step) The default is 33dB

8.1.6.12. 0x0C Left ADC Mixer Source Control Register (Default Value: 0x00)

Offset:0x0C			**Register Name: LADCMIXSC**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control 0: Mute 1: Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: / Bit 3:/ Bit 2: LINEINL Bit 1: Left Output Mixer Bit 0: Right Output Mixer

8.1.6.13. 0x0D Right ADC Mixer Source Control Register (Default Value: 0x00)

Offset:0x0D			**Register Name: RADCMIXSC**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control 0: Mute 1: Not Mute

			Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: / Bit 3:/ Bit 2: LINEINR Bit 1: Right Output Mixer Bit 0: Left Output Mixer

8.1.6.14. 0x0E Reserved Register (Default Value: 0x04)

Offset:0x0E			**Register Name: Res_Reg**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	/	/	/
5:4	R/W	0x0	MBIASSEL MMICBIAS Voltage Level Select 00: 2.068V 01: 2.299V 10: 2.563V 11: 2.73V
3	/	/	/
2:0	R/W	0x4	PA_ANTI_POP PA ANTI-POP Time Control 000: 131ms 001: 262ms 010: 393ms 011: 524ms 100: 655ms 101: 786ms 110: 917ms 111: 1048ms

8.1.6.15. 0x0F ADC Analog Part Enable Register (Default Value: 0x03)

Offset:0x0F			**Register Name: ADC_AP_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	ADCREN ADC Right Channel Enable 0: Disable 1: Enable

6	R/W	0x0	ADCLEN ADC Left Channel Enable 0: Disable 1: Enable
5:3	/	/	/
2:0	R/W	0x3	ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step . The default is 0dB

8.1.6.16. 0x10 ADDA Analog Performance Turning 0 Register (Default Value: 0x55)

Offset:0x10			**Register Name: ADDA_APT0**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x1	OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting
5:4	R/W	0x1	OPADC1_BIAS_CUR. OPADC1 Bias Current Select
3:2	R/W	0x1	OPADC2_BIAS_CUR. OPADC2 Bias Current Select
1:0	R/W	0x1	OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select

8.1.6.17. 0x11 ADDA Analog Performance Turning 1 Register (Default Value: 0x45)

Offset:0x11			**Register Name: ADDA_APT1**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x1	OPMIC_BIAS_CUR OPMIC Bias Current Control
5:4	/	/	/
3:2	R/W	0x1	OPDAC_BIAS_CUR. OPDAC Bias Current Control
1:0	R/W	0x1	OPMIX_BIAS_CUR. OPMIX/OPLPF Bias Current Control

8.1.6.18. 0x12 ADDA Analog Performance Turning 2 Register (Default Value: 0x42)

Offset:0x12			**Register Name: ADDA_APT2**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	Function enable for master volume change at zero cross over

			0: Disable 1: Enable
6	R/W	0x1	Timeout control for master volume change at zero cross over 0: 32ms 1: 64ms
5:4	R/W	0x0	PTDBS HPCOM protect de-bounce time setting 00: 2-3ms 01: 4-6ms 10: 8-12ms 11: 16-24ms At the same time, bit 17 is used to control the AVCCPORFLAG, writing 1 to this bit, the flag will be cleared, and the calibration is done again.
3	R/W	0x0	PA_SLOPE_SELECT PA slope select cosine or ramp 0: Select cosine 1: Select ramp
2:0	R/W	0x2	USB_BIAS_CUR. USB bias current tuning From 23uA to 30uA, the default value is 25uA

8.1.6.19. 0x13 Bias & DA16 Calibration Control Register0 (Default Value: 0xD6)

Offset:0x13			**Register Name: Bias_DA16_CAL_CTR0**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x1	MMIC BIAS Chopper Enable 0: Disable 1: Enable
6:5	R/W	0x2	MMIC BIAS Chopper Clock Select 00: 250KHz 01: 500KHz 10: 1MHz 11: 2MHz
4	R/W	0x1	DITHER ADC Dither on/off Control 0: Dither off 1: Dither on

3:2	R/W	0x1	DITHER_CLK_SELECT ADC Dither Clock Select 00: ADC FS * (8/9), about 43KHz when FS=48KHz 01: ADC FS * (16/15), about 51KHz when FS=48KHz 10: ADC FS * (4/3), about 64KHz when FS=48KHz 11: ADC FS * (16/9), about 85KHz when FS=48KHz
1:0	R/W	0x2	BIHE_CTRL BIHE Control 00: No BIHE 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC

8.1.6.20. 0x14 Bias & DA16 Calibration Control Register1 (Default Value: 0x00)

Offset:0x14			**Register Name: Bias_DA16_CAL_CTR1**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	PA_SPEED_SELECT PA Setup Speed Control (for testing) 0: Slow 1: Fast
6	R/W	0x0	CURRENT_TEST_SELECT Internal Current Sink Test Enable (from LINEIN pin) 0: Normal 1: For Debug
5	R/W	0x0	/
4	R/W	0x0	BIAS and DA16 Calibration Clock Select 0: 1KHz 1: 500Hz
3	R/W	0x0	BIAS Calibration Mode Select 0: Average 1: Single
2	R/W	0x0	BIAS and DA16 Calibration Control Write 1 to this bit, the calibration will be done again. Then this bit will reset to zero automatically
1	R/W	0x0	BIASCALIVERIFY Bias Calibration Verify

			0: Calibration 1: Register setting
0	R/W	0x0	DA16CALIVERIFY DA16 Calibration Verify 0: Calibration 1: Register setting

8.1.6.21. 0x15 DA16 Calibration Data Register (Default Value: 0x80)

Offset:0x15			**Register Name: DA16CALI**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x80	DA16CALI DA16 Calibration Data

8.1.6.22. 0x16 DA16 Register Setting Data Register (Default Value: 0x80)

Offset:0x16			**Register Name: DA16VERIFY**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R/W	0x80	/

8.1.6.23. 0x17 Bias Calibration Data Register (Default Value: 0x20)

Offset:0x17			**Register Name: BIASCALI**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x20	BIASCALI Bias Calibration Data, 6bit

8.1.6.24. 0x18 Bias Register Setting Data Register (Default Value: 0x20)

Offset:0x18			**Register Name: BIASVERIFY**
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R/W	0x20	BIASVERIFY Bias Register Setting Data, 6bit

8.2. I2S/PCM

8.2.1. Overview

The I2S/PCM Controller has been designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified Mode format, Right-justified Mode format, PCM Mode format and TDM Mode format. The I2S/PCM provides a serial bus interface for stereo and multichannel audio data. This interface is most commonly used by consumer audio market, including compact disc, digital audio tape, digital sound processors, and digital TV-sound.

Features:

- Compliant with standard Inter-IC sound(I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode and TDM(Time Division Multiplexing) format
- Supports 8-channel in TDM mode
- Supports full-duplex synchronous work mode
- Supports Master/Slave mode
- Supports adjustable interface voltage
- Supports clock up to 100MHz
- Supports adjustable audio sample rate from 8-bit to 32-bit.
- Supports up to 8 slots which has adjustable width from 8-bit to 32-bit.
- Supports sample rate from 8KHz to 192KHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 x 32-bit width FIFO for data transmit, one 64 x 32-bit width FIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Supports loopback mode for test

8.2.2. Block Diagram

The I2S/PCM interface block diagram is shown below.

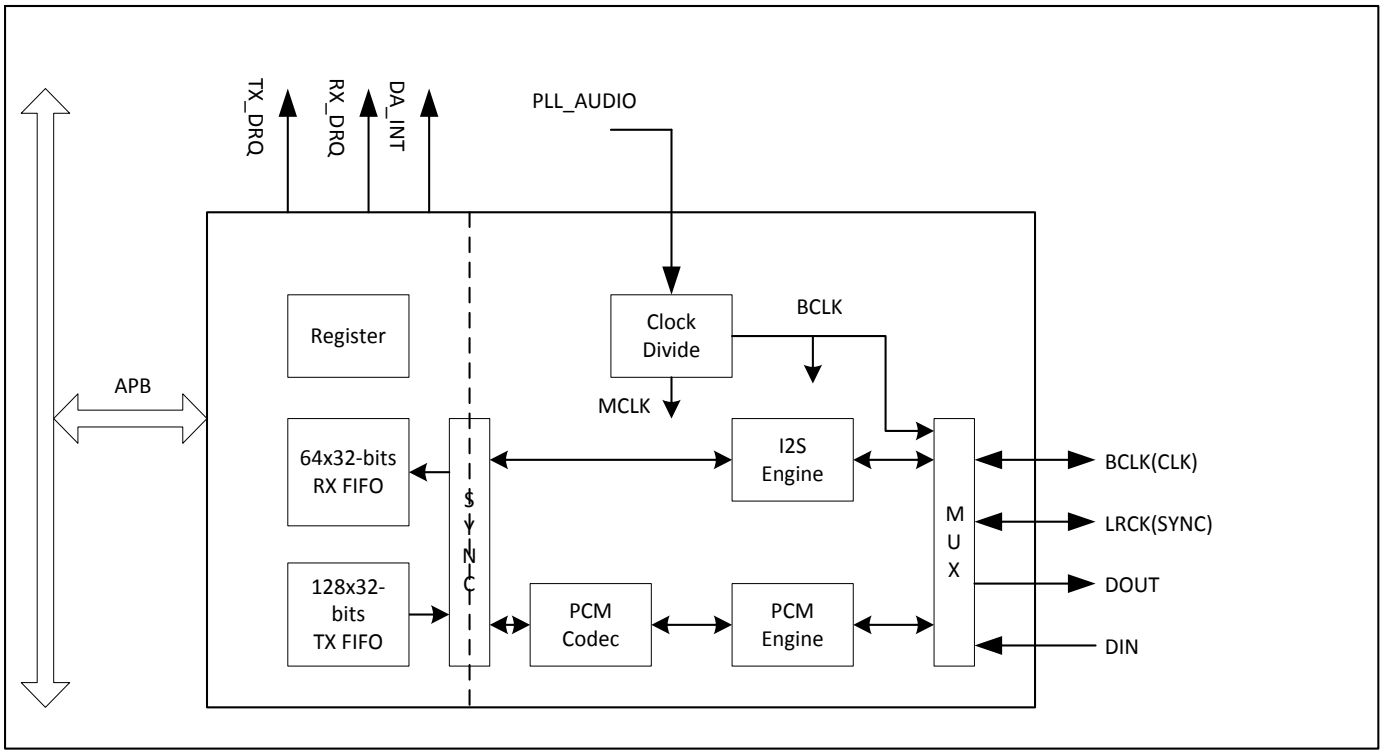


Figure 8-7. I2S/PCM Interface System Block Diagram

8.2.3. Operations and Functional Descriptions

8.2.3.1. External Signals

Table 8-2 describes the external signals of I2S/PCM interface. SYNC and CLK are bidirectional I/O, when I2S/PCM interface is configured as Master device, SYNC and CLK is output pin; when I2S/PCM interface is configured as slave device, SYNC and CLK is input pin. MCLK is an output pin for external device. DOUT is always the serial data output pin, and DIN is the serial data input. For information about General Purpose I/O port, see **Port Controller**.

Table 8-2. I2S/PCM External Signals

Signal Name	Description	Type
PCM0_MCLK	I2S/PCM 0 Master Clock	O
PCM0_CLK	I2S/PCM 0 Sample Rate Serial Clock	I/O
PCM0_SYNC	I2S/PCM 0 Sample Rate Left and Right Channel Select Clock/Sync	I/O
PCM0_DIN	I2S/PCM 0 Serial Data Input	I
PCM0_DOUT	I2S/PCM 0 Serial Data Output	O
PCM1_CLK	I2S/PCM 1 Sample Rate Serial Clock	I/O
PCM1_SYNC	I2S/PCM 1 Sample Rate Left and Right Channel Select Clock/Sync	I/O
PCM1_DIN	I2S/PCM 1 Serial Data Input	I

PCM1_DOUT	I2S/PCM 1 Serial Data Output	O

8.2.3.2. Clock Sources

Table 8-3 describes the clock sources for I2S/PCM. Users can see **Chapter 4.3.CCU** for clock setting, configuration and gating information.

Table 8-3. I2S/PCM Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

8.2.3.3. Timing Diagram

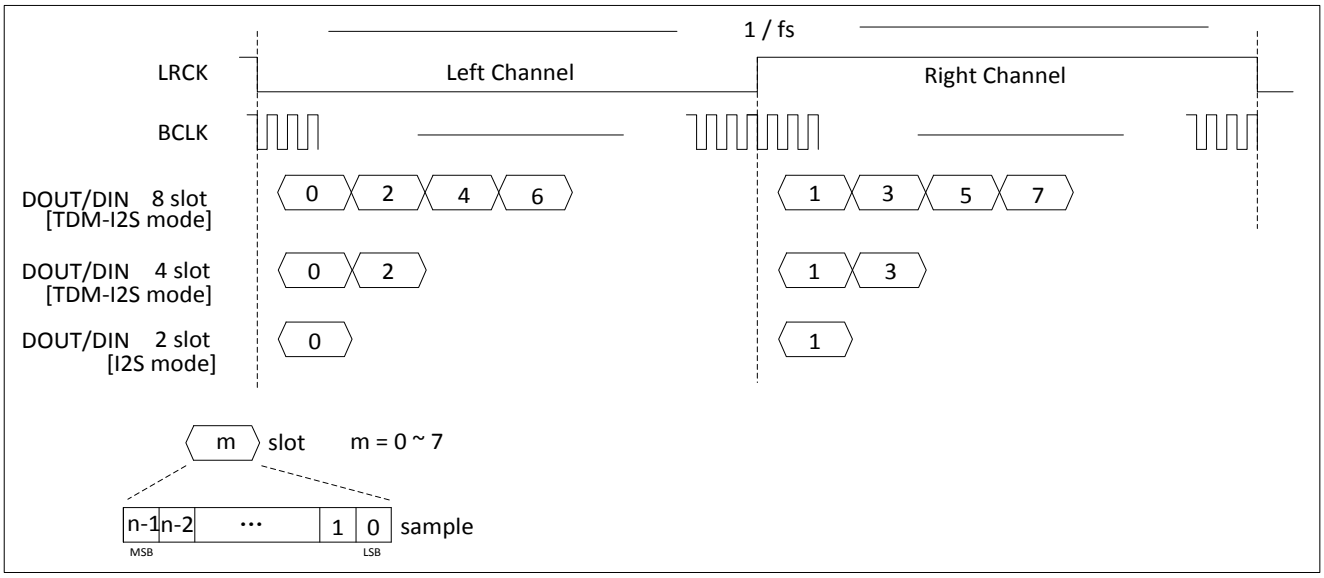


Figure 8-8. I2S/TDM-I2S Mode Timing

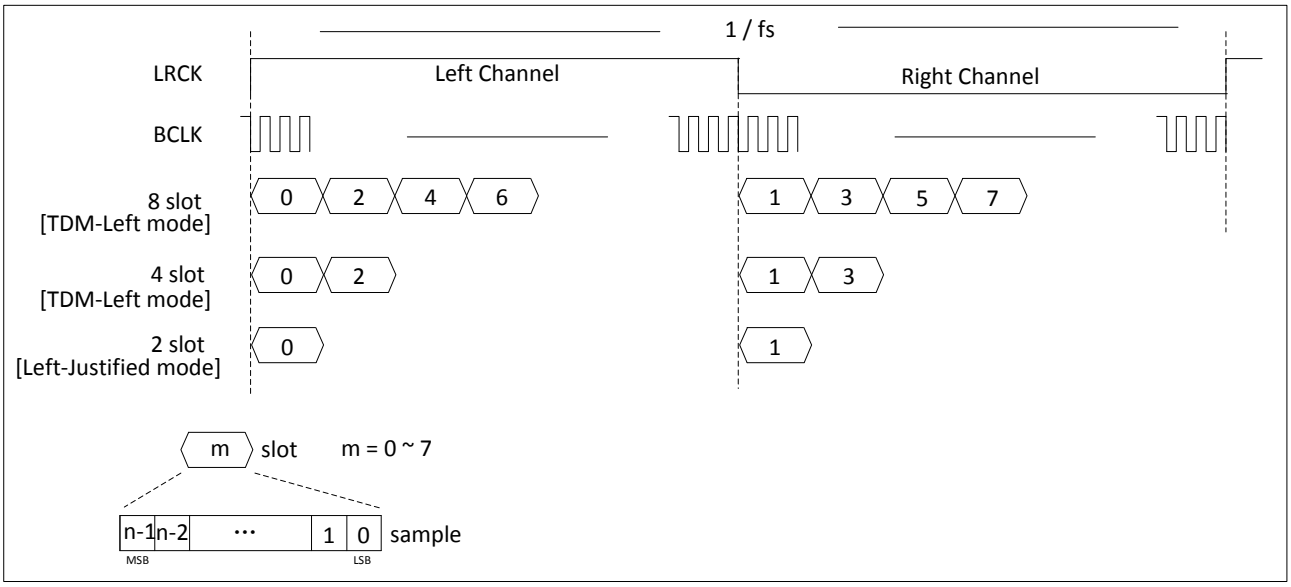


Figure 8-9. Left-Justified/TDM-Left Mode Timing

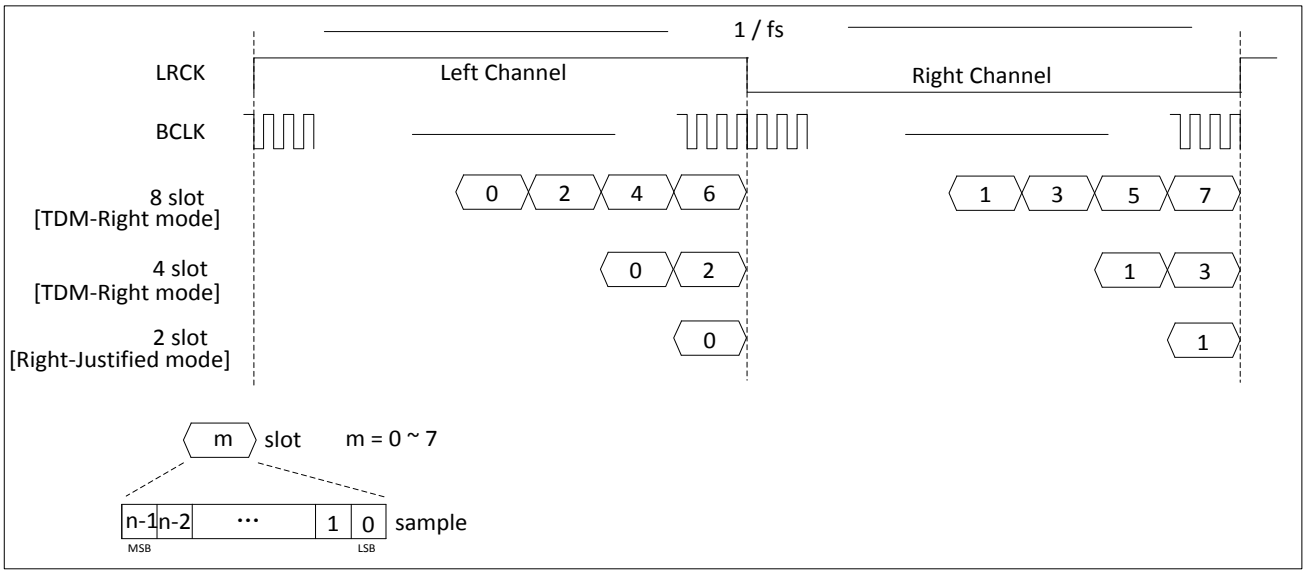


Figure 8-10. Right-Justified/TDM-Right Mode Timing

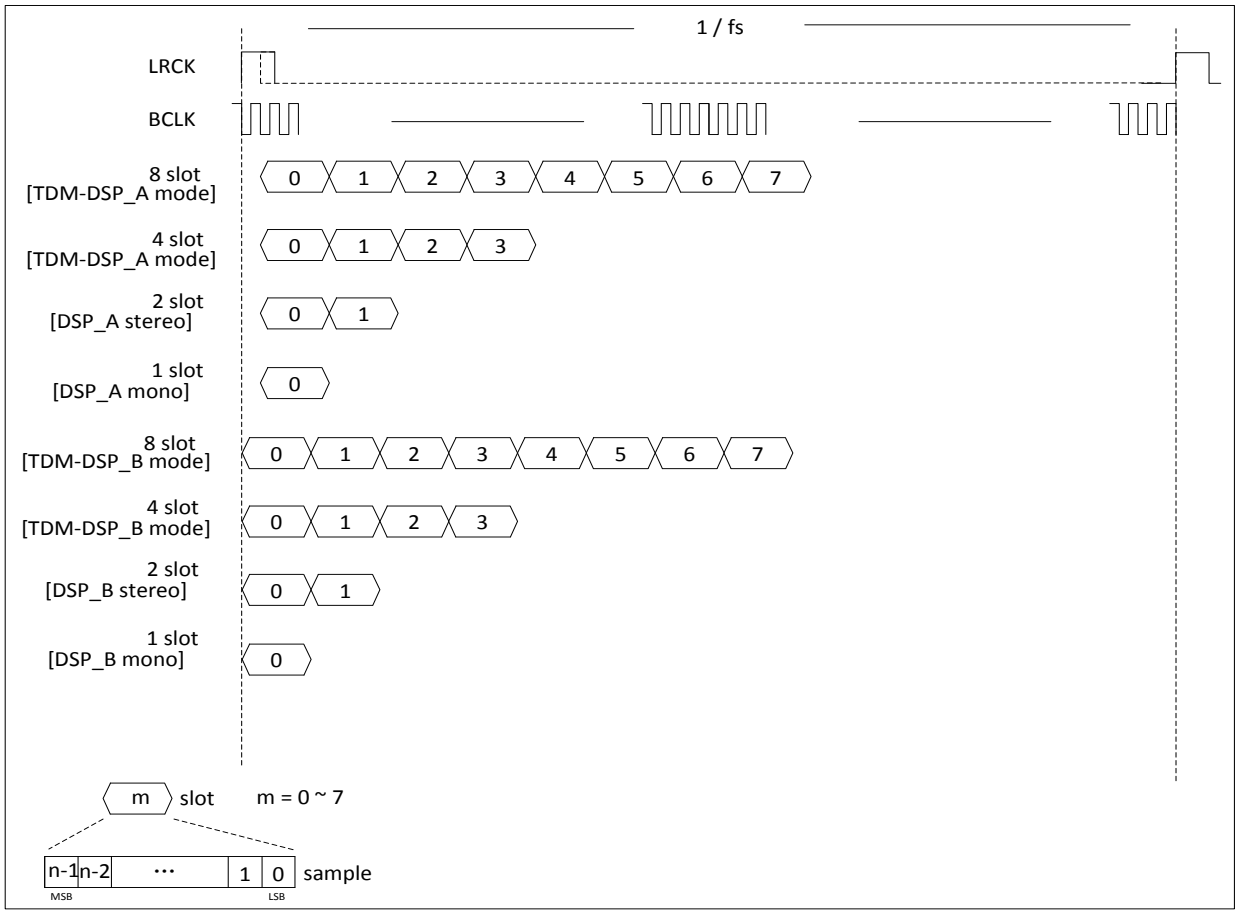


Figure 8-12. Timing Diagram for PCM/TDM-PCM Mode

8.2.3.4. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

(1). System setup and I2S/PCM initialization

The first step in the system setup is properly programming the GPIO. Because the I2S/PCM port is a multiplex pin. You can find the function in **Port Controller(CPUx-PORT)**. The clock source for the I2S/PCM should be followed. At first you must reset the audio PLL though the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG** in the **Chapter 4.3.CCU**. The second step, you must setup the frequency of the audio PLL in the **PLL_AUDIO_CTRL_REG**. After that, you must open the I2S/PCM gating though the **I2S/PCM0_CLK_REG**/**I2S/PCM1_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes to 1. At last, you must reset the I2S/PCM by the bit[13:12] of **BUS_SOFT_RST_REG3** and open the I2S/PCM bus gating by the bit[13:12] of **BUS_CLK_GATING_REG2**.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the **Globe Enable** bit(I2S/PCM_CTL[0]) , **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit[25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to **I2S/PCM_TXCNT** and **I2S/PCM_RXCNT**.

(2). Channel setup and DMA setup

Before the usage and control of I2S/PCM, you must configure the I2C. The configuration of I2C will not describe in this chapter. But you can only configure I2S/PCM of master and slave through the I2C. The configuration can be referred to the protocol of I2S/PCM. Then, you can set the translation mode, the sample precision, the wide of slot, the frame mode and the trigger level.

The I2S/PCM supports three methods to transfer the data. The most common way is DMA, the set of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3). Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing the bit[2:1] of **I2S/PCM_CTL**. After that, you must enable I2S/PCM by writing the **Globe Enable** bit to 1. Writing the **Globe Enable** bit to 0 to disable I2S/PCM.

8.2.4. I2S/PCM Register List

Module Name	Base Address
I2S/PCM 0	0x01C22000
I2S/PCM 1	0x01C22400
I2S/PCM 2	0x01C22800 (for HDMI)

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RX FIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TX FIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TX0CHCFG	0x0034	I2S/PCM TX0 Channel Configuration Register
I2S/PCM_TX1CHSEL	0x0038	I2S/PCM TX1 Channel Select Register
I2S/PCM_TX2CHSEL	0x003C	I2S/PCM TX2 Channel Select Register
I2S/PCM_TX3CHSEL	0x0040	I2S/PCM TX3 Channel Select Register

I2S/PCM_TX0CHMAP	0x0044	I2S/PCM TX0 Channel Mapping Register
I2S/PCM_TX0CHMAP	0x0048	I2S/PCM TX1 Channel Mapping Register
I2S/PCM_TX0CHMAP	0x004C	I2S/PCM TX2 Channel Mapping Register
I2S/PCM_TX0CHMAP	0x0050	I2S/PCM TX3 Channel Mapping Register
I2S/PCM_RXCHSEL	0x0054	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP	0x0058	I2S/PCM RX Channel Mapping Register

8.2.5. I2S/PCM Register Description

8.2.5.1. I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			**Register Name: I2S/PCM_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16	R/W	0x0	LRCKR_OUT 0: Input 1: Output
15:9	/	/	/
8	R/W	0x0	DOUT_EN 0: Disable, Hi-Z state 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE 0: Normal transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM mode (offset 0: DSP_B; offset 1: DSP_A) 01: Left mode (offset 0: LJ mode; offset 1: I2S mode) 10: Right-Justified mode 11: Reserved

3	R/W	0x0	LOOP Loop Back Test 0: Normal mode 1: Loop back test When set '1', connecting the DOUT with the DIN
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

8.2.5.2. I2S/PCM Format Register0(Default Value: 0x0000_0033)

Offset: 0x0004			**Register Name: I2S/PCM_FMT0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH LRCK Width(only apply in PCM mode) 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge

18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S/Left-Justified/Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width … n = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, DOUT drive data at negative edge 1: Invert mode, DOUT drive data at positive edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: DOUT drive data and DIN sample data at the different BCLK edge 1: DOUT drive data and DIN sample data at the same BCLK edge **BCLK_POLARITY** = 0, **EDGE_TRANSFER** = 0, DIN sample data at positive edge **BCLK_POLARITY** = 0, **EDGE_TRANSFER** = 1, DIN sample data at negative edge **BCLK_POLARITY** = 1, **EDGE_TRANSFER** = 0, DIN sample data at negative edge **BCLK_POLARITY** = 1, **EDGE_TRANSFER** = 1, DIN sample data at positive edge
2:0	R/W	0x3	SW Slot Width Select 000: Reserved

			001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

8.2.5.3. I2S/PCM Format Register1(Default Value: 0x0000_0030)

Offset: 0x0008			**Register Name: I2S/PCM_FMT1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	
7	R/W	0x0	RX MLS RX MSB / LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS TX MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [sample resolution < slot width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

8.2.5.4. I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt.
4	R/W1C	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt when data in TXFIFO are less than TX trigger level Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write 1 to clear this interrupt
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt

0	R/W1C	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ when data in RXFIFO are more than RX trigger level Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

8.2.5.5. I2S/PCM RX FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: I2S/PCM_RXFIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

8.2.5.6. I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)

Offset: 0x0014			**Register Name: I2S/PCM_FCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0:Disable 1:Enable
30:26	/	/	/
25	R/W	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
24	R/W	0x0	FRX Write '1' to flush RXFIFO, self clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1

3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1:TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of **I2S/PCM_RXFIFO** register. 01: Expanding received sample sign bit at MSB of **I2S/PCM_RXFIFO** register. 10: Truncating received samples at high half-word of **I2S/PCM_RXFIFO** register and low half-word of **I2S/PCM_RXFIFO** register is filled by '0'. 11: Truncating received samples at low half-word of **I2S/PCM_RXFIFO** register and high half-word of **I2S/PCM_RXFIFO** register is expanded by its sign bit. Example for 20-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12'h0} Mode 1: APB_RDATA [31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16'h0} Mode 3: APB_RDATA [31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

8.2.5.7. I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			**Register Name: I2S/PCM_FSTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available

			0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 word)
7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

8.2.5.8. I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: I2S/PCM_INT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA Request line is asserted if Data is available in RX FIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable

			0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

8.2.5.9. I2S/PCM TX FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

8.2.5.10. I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **Note:** Whether in slave or master mode, when this bit is set to 1, MCLK should output.
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4

			0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

8.2.5.11. I2S/PCM TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

8.2.5.12. I2S/PCM RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by RXFIFO, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

8.2.5.13. I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half cycle of BCLK in the slot 1: Turn to hi-z state for the last half cycle of BCLK in the slot
8	R/W	0x0	TX_STATE 0: Transfer level 0 when not transferring slot 1: Turn to hi-z state when not transferring slot
7	/	/	/
6:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot Number between CPU/DMA and FIFO 000: 1 channel or slot ... 111: 8 channels or slots
3	/	/	/
2:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot Number between CPU/DMA and FIFO 000: 1 channel or slot ... 111: 8 channels or slots

8.2.5.14. I2S/PCM TX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034	Register Name: I2S/PCM_TXCHSEL

Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x0	TX_OFFSET TX offset tune, TX data offset to LRCK 00: No offset 01: Data is offset by 1 BCLKs to LRCK Others: Reserved
11:4	R/W	0x0	TX_CHEN TX Channel (slot) enable, bit[11:4] refer to slot [7:0]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state. 0: Disable 1: Enable
3	/	/	/
2:0	R/W	0x0	TX_CHSEL TX Channel (slot) number select for each output 000: 1 channel / slot … 111: 8 channels / slots

8.2.5.15. I2S/PCM TX Channel Mapping Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	TX_CH7_MAP TX Channel7 Mapping 000: 1st sample … 111: 8th sample
27	/	/	/
26:24	R/W	0x0	TX_CH6_MAP TX Channel6 Mapping 000: 1st sample … 111: 8th sample
23	/	/	/
22:20	R/W	0x0	TX_CH5_MAP TX Channel5 Mapping

			000: 1st sample … 111: 8th sample
19	/	/	/
18:16	R/W	0x0	TX_CH4_MAP TX Channel4 Mapping 000: 1st sample … 111: 8th sample
15	/	/	/
14:12	R/W	0x0	TX_CH3_MAP TX Channel3 Mapping 000: 1st sample … 111: 8th sample
11	/	/	/
10:8	R/W	0x0	TX_CH2_MAP TX Channel2 Mapping 000: 1st sample … 111: 8th sample
7	/	/	/
6:4	R/W	0x0	TX_CH1_MAP TX Channel1 Mapping 000: 1st sample … 111: 8th sample
3	/	/	/
2:0	R/W	0x0	TX_CH0_MAP TX Channel0 Mapping 000: 1st sample … 111: 8th sample

8.2.5.16. I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S/PCM_RXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/

13:12	R/W	0x0	RX_OFFSET RX offset tune, RX data offset to LRCK 00: No offset 01: Data is offset by 1 BCLKs to LRCK Others: Reserved
11:3	/	/	
2:0	R/W	0x0	RX_CHSEL RX channel (slot) number select for input 000: 1 channel / slot … 111: 8 channels / slots

8.2.5.17. I2S/PCM RX Channel Mapping Register(Default Value: 0x0000_0000)

Offset: 0x0058			**Register Name: I2S/PCM_RXCHMAP**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	RX_CH7_MAP RX Channel7 Mapping 000: 1st sample … 111: 8th sample
27	/	/	/
26:24	R/W	0x0	RX_CH6_MAP RX Channel6 Mapping 000: 1st sample … 111: 8th sample
23	/	/	/
22:20	R/W	0x0	RX_CH5_MAP RX Channel5 Mapping 000: 1st sample … 111: 8th sample
19	/	/	/
18:16	R/W	0x0	RX_CH4_MAP RX Channel4 Mapping 000: 1st sample

			… 111: 8th sample
15	/	/	/
14:12	R/W	0x0	RX_CH3_MAP RX Channel3 Mapping 000: 1st sample … 111: 8th sample
11	/	/	/
10:8	R/W	0x0	RX_CH2_MAP RX Channel2 Mapping 000: 1st sample … 111: 8th sample
7	/	/	/
6:4	R/W	0x0	RX_CH1_MAP TX Channel1 Mapping 000: 1st sample … 111: 8th sample
3	/	/	/
2:0	R/W	0x0	RX_CH0_MAP RX Channel0 Mapping 000: 1st sample … 111: 8th sample

8.3. OWA

8.3.1. Overview

The OWA(One Wire Audio) provides a serial bus interface for audio data between system. This interface is widely used for consumer audio.

Features:

- IEC-60958 transmitter functionality
- Compliance with S/PDIF Interface
- Support channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 32×24bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

8.3.2. Block Diagram

The OWA block diagram is shown below.

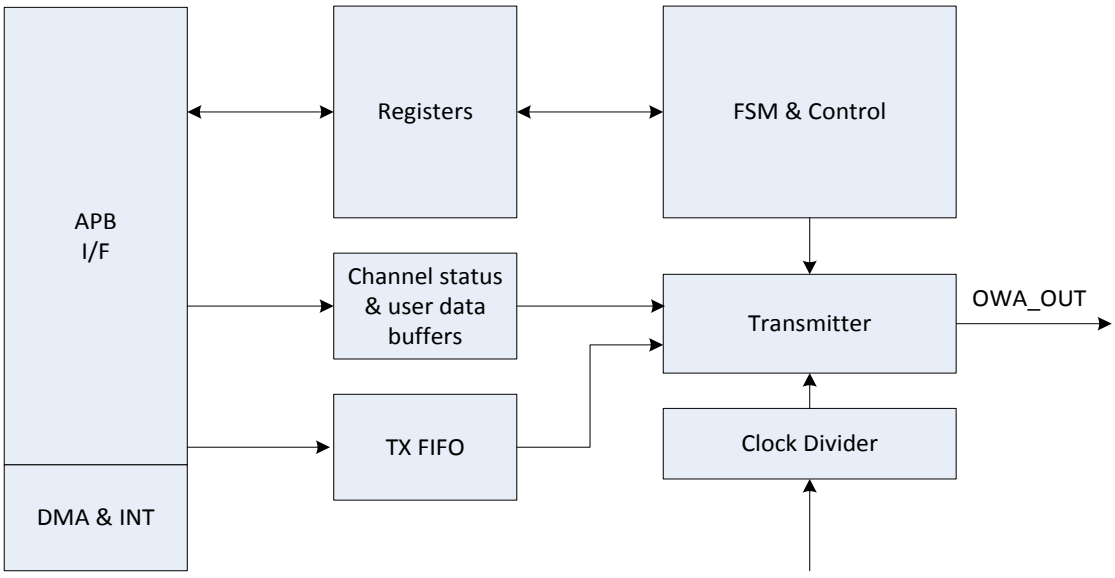


Figure 8-11. OWA Block Diagram

8.3.3. Operations and Functional Descriptions

8.3.3.1. External Signals

Table 8-4 describes the external signals of I2S/PCM interface.

Table 8-4. OWA External Signals

Signal Name	Description	Type
OWA_OUT	OWA output	O

8.3.3.2. Clock Sources

Table 8-5 describes the clock sources for OWA. Users can see **Chapter 4.3.CCU** for clock setting, configuration and gating information.

Table 8-5. OWA Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

8.3.3.3. OWA Frame Format

The OWA supports the transfer of digital audio data. And it supports full-duplex synchronous work mode.

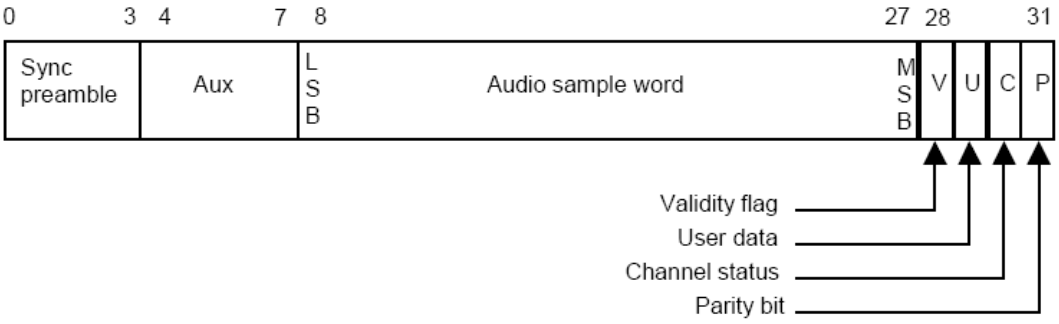


Figure 8-12. Sub-Frame Format

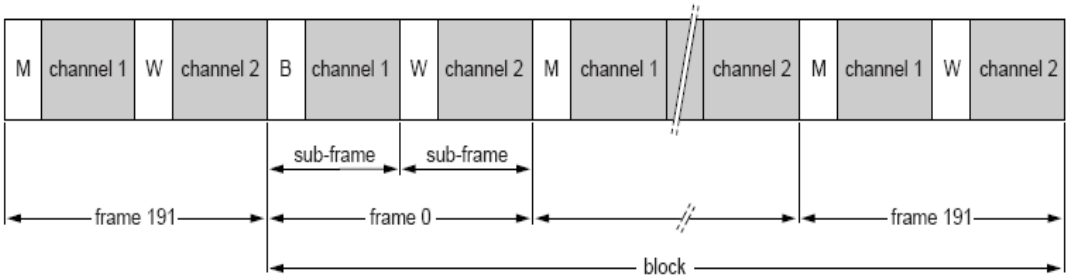


Figure 8-13. Frame/Block Format

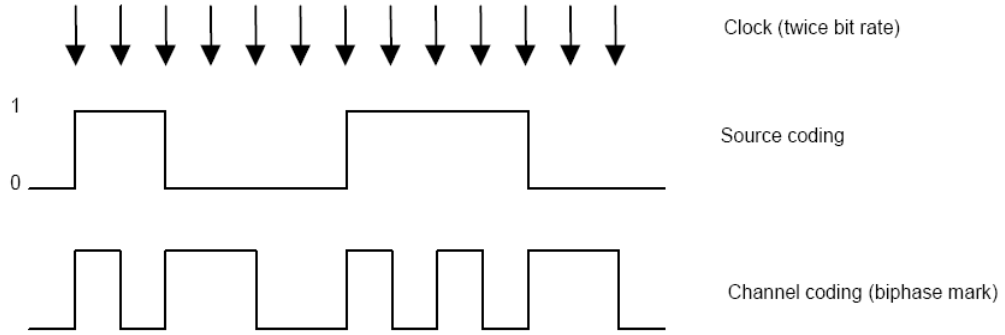


Figure 8-14. Biphase-Mark Encoding

8.3.3.4. Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, the channel setup, DMA setup and enable/disable module. These five steps are described in detail in the following sections.

(1) System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO. Because the OWA port is a multiplex pin. You can find the function in the **Port Controller**. The clock source for the OWA should be followed. At first you must reset the audio PLL in the **CCU**. The second step, you must setup the frequency of the Audio PLL. After that, you must open the OWA gating. At last, you must open the OWA bus gating.

After the system setup, the register of OWA can be setup. At first, you should reset the OWA by writing 1 to **OWA_CTL**[0] and clear the TX FIFO by writing 1 to **OWA_FCTL**[17:16]. After that you should enable the globe enable bit by writing 1 to **OWA_CTL**[1] and clear the interrupt and TX counter by the **OWA_ISTA** and **OWA_TX_CNT**.

(2) Channel Setup and DMA Setup

The OWA support three methods to transfer the data. The most common way is DMA, the configuration of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3) Enable and Disable OWA

To enable the function, you can enable TX by writing the **OWA_TX_CFIG**[31]. After that, you must enable OWA by writing the **GEN** bit to 1 in the **OWA_CTL** register. Writing the **GEN** bit to 0 disable process.

8.3.4. Register List

Module Name	Base Address
OWA	0x01C21000

Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1

8.3.5. Register Description

8.3.5.1. OWA General Control Register (Default Value : 0x0000_0000)

Offset: 0x0000			Register Name: OWA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
0	R/W	0x0	RST Reset 0: Normal

			1: Reset Self clear to 0.

8.3.5.2. OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_SINGLE_MODE Tx Single Channel Mode 0: Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select with TX FIFO Underrun When 0: Sending 0 1: Sending the last audio This bit is only valid in PCM mode
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio(Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX Clock Divide Ratio Clock divide ratio = TX TATIO +1
3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A&B set to 0 1: Channel status A&B generated form TX_CHSTA
0	R/W	0x0	TXEN 0: Disabled

			1: Enabled

8.3.5.3. OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			**Register Name: OWA_ISTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: FIFO Underrun Pending Interrupt Writing “1” to clear this interrupt
5	R/W	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Writing “1” to clear this interrupt
4	R/W	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Writing “1” to clear this interrupt or automatically clear if the interrupt condition fails.
3:0	/	/	/

8.3.5.4. OWA FIFO Control Register (Default Value: 0x0000_1078)

Offset: 0x0014			**Register Name: OWA_FCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	FTX Writing “1” to flush TX FIFO, self clear to “0”

16:13	/	/	/
12:8	R/W	0x10	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition Trigger Level = TXTL
7:3	R/W	0x0F	/
2	R/W	0x0	TXIM TX FIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of OWA_TXFIFO register 1: Valid data at the LSB of OWA_TXFIFO register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[23:0] = {APB_WDATA[31:12], 4'h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4'h0}
1:0	/	/	/

8.3.5.5. OWA FIFO Status Register (Default Value: 0x0000_6000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R	0x1	TXE TX FIFO Empty (indicate FIFO is not full) 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>=1 word)
13:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:0	/	/	/

8.3.5.6. OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TX FIFO Underrun Interrupt Enable

			0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3:0	/	/	/

8.3.5.7. OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. The A channel data is first and then the B channel data.

8.3.5.8. OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After updated by the initial value, the counter register should count on base of this initial value.

8.3.5.9. OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy

			00: Level 2 01: Level 1 10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1kHz 0001: Not indicated 0010: 48kHz 0011: 32kHz 0100: 22.05kHz 0101: Reserved 0110: 24kHz 0111: Reserved 1000: Reserved 1001: 768kHz 1010: 96kHz 1011: Reserved 1100:176.4kHz 1101: Reserved 1110: 192kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 µs / 15 µs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis)

			011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = "1", other than Linear PCM applications: 000: Default state 001~111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM Samples 1: For none-linear PCM audio such as AC3, DTS, MPEG audio
0	R/W	0x0	PRO Application Type 0: Consumer Application 1: Professional Application This bit must be fixed to "0"

8.3.5.10. OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			**Register Name: OWA_TX_CHSTA1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz

			0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = “0”: 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

Chapter 9 Interfaces

This chapter describes the H5 interfaces, including:

- TWI
- SPI
- UART
- CIR Receiver
- USB
- SCR
- EMAC
- TSC

9.1. TWI

9.1.1. Overview

This TWI controller is designed to be used as an interface between CPU host and the serial 2-wire bus. It can support all the standard 2-wire transfer, including slave and master. The communication of the 2-wire bus is carried out by a byte-wise mode based on interrupt or polled handshaking. This TWI controller can be operated in standard mode (100 Kbit/s) or fast-mode, supporting data rate up to 400 Kbit/s. Multi-masters and 10-bit addressing mode are supported for this specified application. General Call Addressing is also supported in slave mode.

Features:

- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speed up to 400 Kbit/s ('fast mode')
- Allows operation from a wide range of input clock frequencies

9.1.2. Operations and Functional Descriptions

9.1.2.1. External Signals

H5 has 3 TWIs in CPUx and 1 TWI in CPUs. Table 9-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O, When TWI is configured as Master device, TWI_SCK is output pin; when TWI is configurable as Slave device, TWI_SCK is input pin. The unused TWI ports are used as General Purpose I/O ports. For information about General Purpose I/O ports, see **Port Controller(CPUx-PORT)** and **Port Controller (CPUs-PORT)** in chapter4.

Table 9-1. TWI External Signals

Port Name	Direction	Description
TWI0_SCK	I/O	TWI0 clock line
TWI0_SDA	I/O	TWI0 serial data signal
TWI1_SCK	I/O	TWI1 clock line
TWI1_SDA	I/O	TWI1 serial data signal
TWI2_SCK	I/O	TWI2 clock line
TWI2_SDA	I/O	TWI2 serial data signal
S_TWI_SCK	I/O	TWI clock line for CPUs

S_TWI_SDA	I/O	TWI serial data signal for CPUs

9.1.2.2. Clock Sources

The clock source of each TWI controller is APB2 bus clock. Users can see **CCU** in chapter4 for clock setting, configuration and gating information.

Table 9-2. TWI Clock Sources

Clock Sources	Description
APB2	APB2 has three clock sources, including LOSC,OSC24M and PLL_PERIPH0(1X)

9.1.2.3. Timing Diagram

Data transferred are always in a unit of 8-bit (1 byte), followed by an acknowledge bit. The number of bytes that can be transmitted is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each byte. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or pull it high to send a "not acknowledge") to the transmitter.

When a slave receiver does not acknowledge the slave address (unable to receive because of no resource available), the data line must be pulled high by the slave so that the master can generate a STOP condition to stop the transfer. When the acknowledge signal is pulled high, slave receiver no longer sends more data. And the master should generate the STOP condition to stop the transfer.

Figure 9-1 provides an illustration the relation of SDA signal line and SCL signal line on the TWI serial bus.

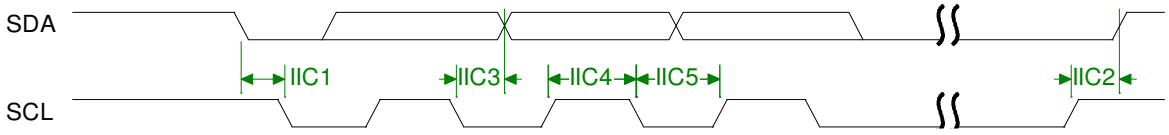


Figure 9-1. TWI Timing Diagram

9.1.2.4. TWI Controller Operation

There are four communication operation modes for the TWI bus, including Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. TWI

transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit to high.

In Slave mode, the TWI also constantly samples the bus and looks for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupted the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

9.1.3. Register List

Module Name	Base Address
R_TWI	0x01F02400
TWI0	0x01C2AC00
TWI1	0x01C2B000
TWI2	0x01C2B400

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address Register
TWI_XADDR	0x0004	TWI Extended Slave Address Register
TWI_DATA	0x0008	TWI Data Byte Register
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset Register
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register

9.1.4. Register Description

9.1.4.1. TWI Slave Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

7:1	R/W	0x0	SLA Slave address • 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 • 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General call address enable 0: Disable 1: Enable

Note:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode (SLA6 corresponds to the first bit received from the TWI bus.). If **GCE** is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match **TWI_ADDR**[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK (The device does not generate an interrupt at this point.). If the next byte of the address matches the **TWI_XADDR** register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

9.1.4.2. TWI Extend Address Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: TWI_XADDR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

9.1.4.3. TWI Data Register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: TWI_DATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte for transmitting or received

9.1.4.4. TWI Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when **INT_FLAG** is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus inputs ISDA/ISCL are ignored and the TWI controller will not respond to any address on the bus 1: The TWI will respond to call to its slave address – and to the general call address if the **GCE** bit in the **TWI_ADDR** register is set. **Note:** In master operation mode, this bit should be set to '1'.
5	R/W	0x0	M_STA Master Mode Start When **M_STA** is set to '1', the TWI controller enters master mode and will transmit a START condition on the bus when the bus is free. If **M_STA** is set to '1' when the TWI controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If **M_STA** is set to '1' when the TWI is accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. **M_STA** is cleared automatically after a START condition sent. Writing a '0' to this bit has no effect.
4	R/W	0x0	M_STP Master Mode Stop If **M_STP** is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If **M_STP** is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both **M_STA** and **M_STP** are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. **M_STP** is cleared automatically. Writing a '0' to this bit has no effect.
3	R/W	0x0	INT_FLAG Interrupt Flag **INT_FLAG** is automatically set to '1' when any of 28 (out of the possible 29)

			states is entered (see '**TWI_STAT**' below). **INT_FLAG** can not be set when TWI code state is F8h. If the **INT_EN** bit is set, the interrupt line goes high when **INT_FLAG** is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when **INT_FLAG** is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to **INT_FLAG**. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When **A_ACK** is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the **GCE** bit in the **TWI_ADDR** register is set to '1'. (3). A data byte has been received in master or slave mode. When **A_ACK** is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If **A_ACK** is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when **INT_FLAG** is cleared. The TWI will not respond as a slave unless **A_ACK** is set.
1:0	/	/	/

9.1.4.5. TWI Status Register(Default Value: 0x0000_00F8)

Offset: 0x0010			**Register Name: TWI_STAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received

			0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, ACK not transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, ACK not transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, ACK not transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

9.1.4.6. TWI Clock Register(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: TWI_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48MHz (APB clock input) For 400KHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48M/2^2=12MHz, F1= F0/(10*(2+1)) = 0.4MHz For 100KHz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48M/2^2=12MHz, F1=F0/(10*(11+1)) = 0.1MHz

9.1.4.7. TWI Soft Reset Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation.

9.1.4.8. TWI Enhance Feature Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	DBN Data Byte number follow Read Command Control 00: No Data Byte to be written after read command 01: Only 1 byte data to be written after read command 10: 2 bytes data can be written after read command 11: 3 bytes data can be written after read command

9.1.4.9. TWI Line Control Register(Default Value: 0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x1	SCL_STATE Current state of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current state of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (**SCL_CTL_EN** is set), this bit decide the

			output level of TWI_SCL. 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is controlled by the value of **SCL_CTL**. 0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (**SDA_CTL_EN** is set), this bit decides the output level of TWI_SDA. 0: Output low level 1: Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is controlled by the value of **SDA_CTL**. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

9.2. SPI

9.2.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with fewer software interrupts. It can interface with up to four slave external devices or one single external master. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode.

Features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive date
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Mode0~3 are supported for both transmit and receive operations
- The maximum frequency is 100MHz
- Interrupt or DMA supported
- Support single and dual read mode

9.2.2. Block Diagram

Figure 9-2 shows a block diagram of the SPI.

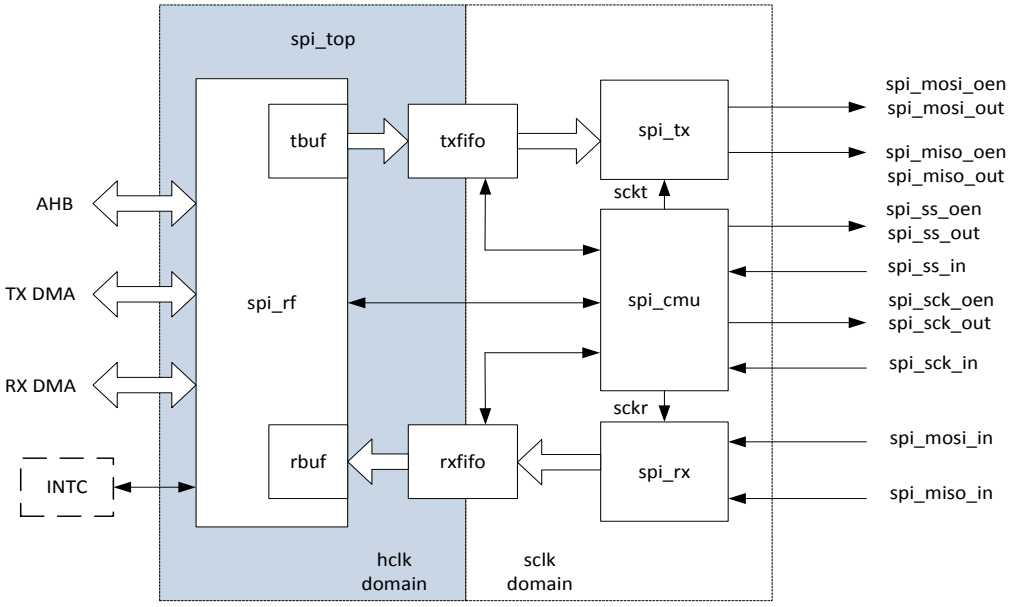


Figure 9-2. SPI Block Diagram

The SPI comprises with:
spi_rf: Responsible for implementing the internal register,interrupt and DMA Request.
spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8bits,then the data is written into the rxfifo.
spi_rbuf: The block is used as converted the rxfifo data into read data length of AHB.
txfifo,rxfifo: For transmit and receive transfers,data transmitted from the SPI to the external serial device is written into the txfifo;data received from the external serial device into SPI is pushed into the rxfifo.
spi_cmu: Responsible for implementing SPI bus clock,chip select,internal sample and the generation of transfer clock.
spi_tx: Responsible for implementing SPI data transfer ,the interface of the internal txfifo and status register.
spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

9.2.3. Operations and Functional Descriptions

9.2.3.1. External Signals

Table 9-3 describes the external signals of SPI. MOSI and MISO are bidirectional I/O, when SPI is configured as Master device, CLK and CS is output pin; when SPI is configurable as Slave device, CLK and CS is input pin. The unused SPI ports are used as General Purpose I/O ports.

Table 9-3. SPI External Signals

Signal	Description	Type
SPI0_CS	SPI0 Chip Select Signal,Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI1_CS	SPI1 Chip Select Signal,Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O

9.2.3.2. Clock Sources

Each SPI controller get three different clocks, users can select one of them to make SPI Clock Source. Table 9-4 describes the clock sources for SPI.

Table 9-4. SPI Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz

9.2.3.3. SPI Transmit Format

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 9-5.

Table 9-5. SPI Transmit Format

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 9-3 and Figure 9-4 describe four waveforms for SPI_SCLK.

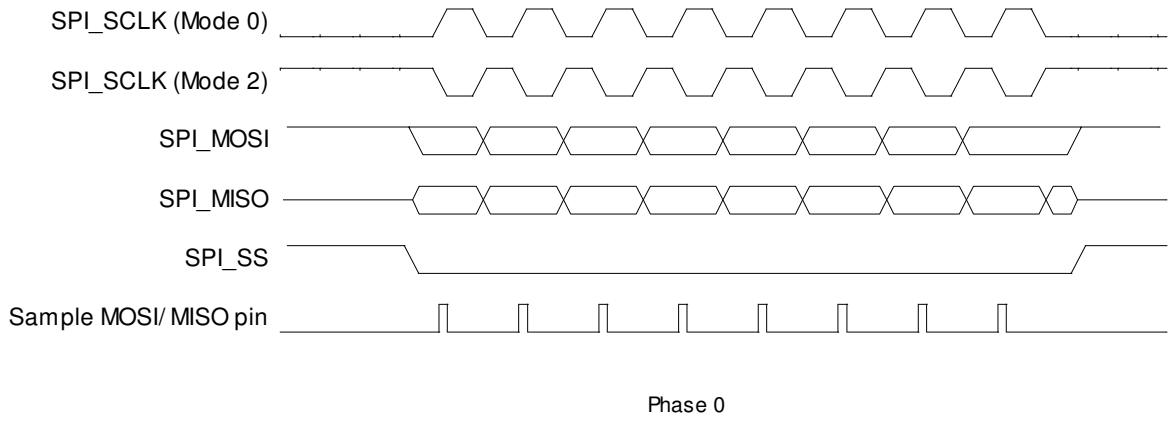


Figure 9-3. SPI Phase 0 Timing Diagram

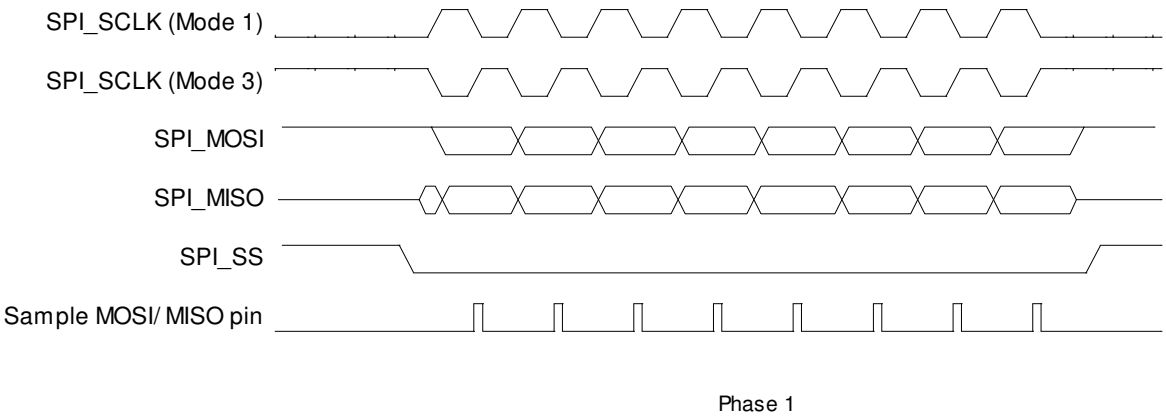


Figure 9-4. SPI Phase 1 Timing Diagram

9.2.3.4. SPI Master and Slave Mode

The SPI controller can be configured to a Master or Slave device. Master mode is selected by setting the **MODE** bit in the **SPI Global Control Register**;Slave mode is selected by clearing the **MODE** bit in the **SPI Global Control Register**.

In Master mode, SPI_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received. SPI_SS can be selected SPI auto control or software manual control. When using auto control,**SS_OWNER** (the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control, **SS_OWNER** must be set, chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In Slave mode, after software selects the **MODE** bit to '0',it waits for master initiate a transaction. When the Master assert SPI_SS and SPI_CLK is transmitted to the Slave ,the Slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

9.2.3.5. SPI Dual Read Mode

The Dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**.Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices, data can be read at fast speed using two data bits(MOSI and MISO) at a time.

9.2.4. Programming Guide

9.2.4.1. Transmit/Receive Burst in Master Mode

In SPI Master mode, the transmit and receive burst(byte in unit) are configured before the SPI transfers serial data

between the processor and external device. The transmit burst write in **MWTC**(bit[23:0]) of **SPI Master Transmit Counter Register**. The transmit burst in single mode before automatically sending dummy burst write in **STC**(bit[23:0]) of **SPI Master Burst Control Counter Register.**For dummy data, SPI controller can automatically sent before receive by writing **DBC**(bit[27:24]) in **SPI Master Burst Control Counter Register**.If users do not use SPI controller to sent automatically dummy, then dummy burst are used as the transmit counters to write together in **MWTC**(bit[23:0]) of **SPI Master Transmit Counter Register**.In Master mode, the total burst numbers write in **MBC**(bit[23:0]) of **SPI Master Burst Counter Register**.When all master transmit burst and receive burst are transferred, SPI controller will send a completed interrupt, at the same time, SPI controller will clear **DBC**, **MWTC** and **MBC**.

9.2.4.2. SPI Sample Mode and Run Clock Configuration

The SPI Controller runs at 3KHz~100MHz at its interface to external SPI devices. The internal SPI Clock should run at the same frequency as the outgoing clock in master mode. The SPI clock is selected different clock sources, SPI must configure different work mode. There are three work mode: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. When SPI runs at 48MHz or below 48MHz, SPI can work at normal sample mode or delay half cycle sample mode. When SPI runs over 48MHz,Set the **SDC** bit in **SPI Transfer Control Register** to '1' to make the internal read sample point with a half cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. The different configuration of SPI sample mode shows in Table 9-6.

Table 9-6. SPI Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24MHz
delay half cycle sample	0	0	<=48MHz
delay one cycle sample	0	1	>=60MHz

9.2.5. Register List

Module Name	Base Address
SPI0	0x01C68000
SPI1	0x01C69000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
/	0x000C	Reserved
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Counter Register
SPI_CCR	0x0024	SPI Clock Rate Control Register

/	0x0028	Reserved
/	0x002C	Reserved
SPI_MBC	0x0030	SPI Burst Counter Register
SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control Register
SPI_NDMA_CTL	0x0088	SPI Normal DMA Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

9.2.6. Register Description

9.2.6.1. SPI Global Control Register(Default Value: 0x0000_0080)

Offset: 0x0004			**Register Name: SPI_GCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Write '1' to this bit will clear the SPI controller, and automatically clear to '0' when reset operation completes. Writing '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 0: Normal operation, ignore RXFIFO status 1: Stop transmit data when RXFIFO full **Note:** Can not be written when XCH=1
6:2	/	/	/
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode **Note:** Can not be written when XCH=1
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable

9.2.6.2. SPI Transfer Control Register(Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write "1" to this bit will start the SPI burst, and will automatically clear after finishing the bursts transfer specified by BC. Write "1" to **SRST** will also clear this bit. Writing '0' to this bit has no effect. **Note:** Can not be written when XCH=1.
30:15	/	/	/
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to '0' to make the data send with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode0.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay Sample Mode 1: Normal Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode. In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first **Note:** Can not be written when XCH=1.
11	R/W	0x0	SDC

			Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point **Note:** Can not be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select Rapids mode for high speed write. 0: Normal write mode 1: Rapids write mode **Note:** Can not be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one **Note:** Can not be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. **Note:** Can not be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high **Note:** Can not be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, the controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write **SS_LEVEL** to 1 or 0 to

			control the level of SS signal. 0: SPI controller 1: Software **Note:** Can not be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note:** Can not be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave for the SPI_SSx signal. Only valid when **SS_OWNER** = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts **Note:** Can not be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note:** Can not be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note:** Can not be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) **Note:** Can not be written when XCH=1.

9.2.6.3. SPI Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN

			TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

9.2.6.4. SPI Interrupt Status Register(Default Value: 0x0000_0032)

Offset: 0x0014			**Register Name: SPI_INT_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by **SPI_BC** have been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed

11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflow
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO is underrun. Writing 1 to this bit clears it. 0: RXFIFO is not underrun 1: RXFIFO is underrun
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO is overflow. Writing 1 to this bit clears it. 0: RXFIFO is not overflow. 1: RXFIFO is overflow.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL

			This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing "1" to this bit clears it. Where TX_WL is the water level of RXFIFO.
3	/	/	Reserved
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing 1 to this bit clears it. Where RX_WL is the water level of RXFIFO.

9.2.6.5. SPI FIFO Control Register(Default Value: 0x0040_0001)

Offset: 0x0018			**Register Name: SPI_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing '1' to this bit will reset the control portion of the TX FIFO and automatically clear to '0' when completing reset operation. Writing to '0' has no effect.
30	R/W	0x0	TF_TEST TX Test Mode Enable 0: Disable 1: Enable **Note:** In normal mode, TX FIFO can only be read by SPI controller, writing '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO. **RF_TEST** and **TF_TEST** can not be set at the same time.
29:26	/	/	/

25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing '1' to this bit will reset the control portion of the receiver FIFO, and automatically clear to '0' when completing reset operation, write '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable **Note:** In normal mode, RX FIFO can only be written by SPI controller, writing '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO. **RF_TEST** and **TF_TEST** can not be set at the same time.
13:9	/	/	/
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

9.2.6.6. SPI FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SPI_FSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter

			These bits indicate the number of words in TX FIFO 00000000: 0 byte in TX FIFO 00000001: 1 byte in TX FIFO … 01000000: 64 bytes in TX FIFO Others: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer.
11:8	R	0x0	Reserved
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 00000000: 0 byte in RX FIFO 00000001: 1 byte in RX FIFO … 01000000:64 bytes in RX FIFO Others: Reserved

9.2.6.7. SPI Wait Clock Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: SPI_WCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted N: N SPI_SCLK wait states inserted **Note:** These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by **SWC** for delaying next word data transfer. These bits can not be written when XCH=1.
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by **WCC** for delaying next word data transfer.

			0: No wait states inserted N: N SPI_SCLK wait states inserted

9.2.6.8. SPI Clock Control Register(Default Value: 0x0000_0002)

Offset: 0x0024			Register Name: SPI_CCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0x0	CDR1 Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / 2^n.
7:0	R/W	0x2	CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(n + 1)).

9.2.6.9. SPI Master Burst Counter Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_BC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts

9.2.6.10. SPI Master Transmit Counter Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_TC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MWTC

			Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

9.2.6.11. SPI Master Burst Control Counter Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: SPI_BCC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode **Note:** Can not be written when XCH=1.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The device does not care the data. 0: 0 burst 1: 1 burst … N: N bursts **Note:** Can not be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts

			Note: Can not be written when XCH=1.

9.2.6.12. SPI Normal DMA Control Register(Default Value: 0x0000_00A5)

Offset: 0x0088			**Register Name: SPI_NDMA_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA5	NDMA_MODE_CTL 0xEA: NDMA handshake mode **Note:** NDMA wait mode does not care the value. 0xA5 can be used in handshake mode, but 0xEA is better.

9.2.6.13. SPI TX Data Register(Default Value: 0x0000_0000)

Offset: 0x0200			**Register Name: SPI_TXD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in RXFIFO, one burst data is written to RXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note:** This address is writing-only if **TF_TEST** is '0', and if **TF_TEST** is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.

9.2.6.14. SPI RX Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			**Register Name: SPI_RXD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4.

			Note: This address is read-only if **RF_TEST** is '0', and if **RF_TEST** is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.

9.3. UART

9.3.1. Overview

The Universal Asynchronous Receiver and Transmitter(UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

H5 has five UARTs named UART0,UART1,UART2,UART3 and R_UART. Each UART performs serial-to -parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the master(CPU).

The interface is fully programmable through 8-bit CPU interface. The registers are 32-bit word aligned. The UARTs can control the character length, baud rate, parity generation/checking, and interrupt generation. It supports word lengths from 5 to 8bits,an optional parity bit, and 1,1.5 or 2 stop bits. If enabled, parity can be odd, even, or no parity. Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

The UARTs support both 16450 and 16550 compatible modes. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled. It also includes a 16-bit programmable baud rate generator and an 8-bit scratch register, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Features:

- Compatible with industry-standard 16550 UARTs
- Supports for word length from 5 to 8 bits, an optional parity bit, and 1,1.5 or 2 stop bits
- Programmable parity(even, odd and no parity)
- 64 bytes transmit and receive data FIFOs
- DMA controller interface
- Software/Hardware flow control
- Programmable Transmit Holding Register Empty Interrupt
- Interrupt support for FIFOs, Status Change

9.3.2. Block Diagram

Figure 9-5 shows a block diagram of the UART.

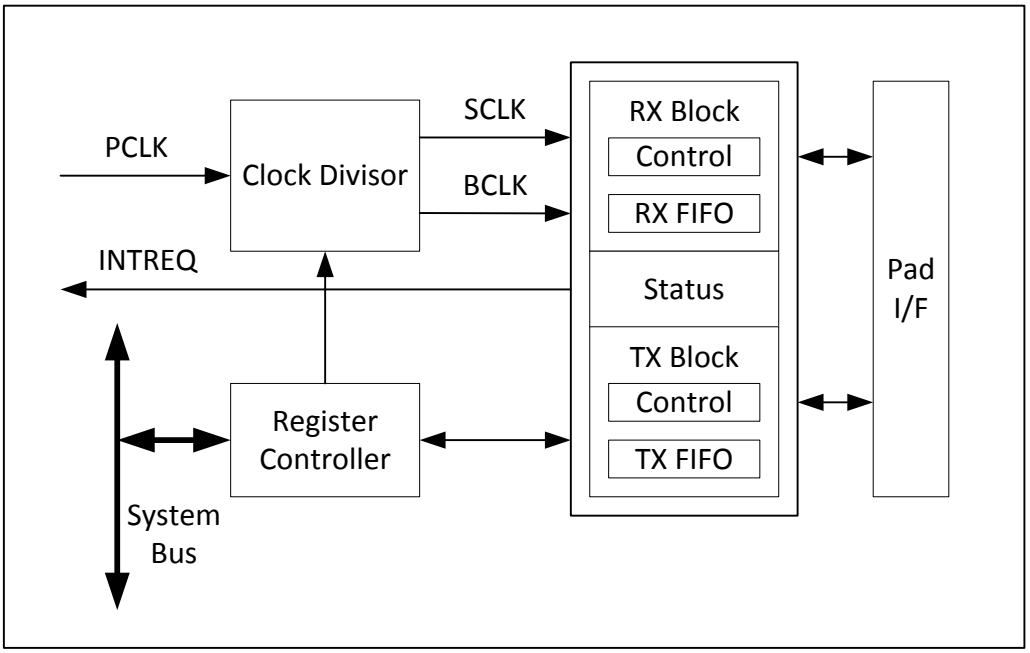


Figure 9-5. UART Block Diagram

9.3.3. Operations and Functional Descriptions

9.3.3.1. External Signals

Table 9-7 describes the external signals of UART.

Table 9-7. UART External Signals

Port Name	Width	Type	Description
UART0_TX	1	O	UART Serial Bit Output
UART0_RX	1	I	UART Serial Bit Input
UART1_TX	1	O	UART Serial Bit Output
UART1_RX	1	I	UART Serial Bit Input
UART1_RTS	1	O	UART Request To Send This active low output signal informs modem that the UART is ready to send data.
UART1_CTS	1	I	UART Clear To End This active low signal is an input signal when modem is ready to accept data.
UART2_TX	1	O	UART Serial Bit Output
UART2_RX	1	I	UART Serial Bit Input
UART2_RTS	1	O	UART Request To Send This active low output signal informs modem that the UART is ready to send data.
UART2_CTS	1	I	UART Clear To End

			This active low signal is an input signal when modem is ready to accept data.
UART3_TX	1	O	UART Serial Bit Output
UART3_RX	1	I	UART Serial Bit Input
UART3_RTS	1	O	UART Request To Send This active low output signal informs modem that the UART is ready to send data.
UART3_CTS	1	I	UART Clear To End This active low signal is an input signal when modem is ready to accept data.
S_UART_TX	1	O	UART Serial Bit Output
S_UART_RX	1	I	UART Serial Bit Input

9.3.3.2. Clock Sources

Table 9-8 describes the clock sources of UART. UART is on APB2 Bus. The clock of APB2 Bus has three sources: LOSC,OSC24M,PLL_PERIPH0(1X).

Table 9-8. UART Clock Sources

Clock Sources		Description
APB2	LOSC	32KHz Crystal
	OSC24M	24MHz Crystal
	PLL_PERIPH0(1X)	Peripheral Clock, default value of 1X is 600MHz

9.3.3.3. UART Timing Diagram

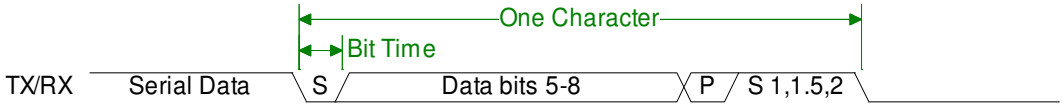


Figure 9-6. UART Serial Data Format

9.3.4. Register List

Module Name	Base Address
UART0	0x01C28000
UART1	0x01C28400
UART2	0x01C28800
UART3	0x01C28C00
R-UART	0x01F02800

Register Name	Offset	Description

UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level
UART_RFL	0x0084	UART Receive FIFO Level
UART_HALT	0x00A4	UART Halt TX Register

9.3.5. Register Description

9.3.5.1. UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: UART_RBR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the **Data Ready** bit in the **UART_LSR** register is set. If in FIFO mode and FIFOs are enabled (**FIFOE** = 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

9.3.5.2. UART Transmit Holding Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: UART_THR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

7:0	W	0x0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to **THR** when the **THRE** bit is set. If in FIFO mode and FIFOs are enabled (**FIFOE** = 1) and **THRE** is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any write data operations when the FIFO is full causes the write data loss.

9.3.5.3. UART Divisor Latch Low Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: UART_DLL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register contains the baud rate divisor for the UART. This register may only be accessed when the **DLAB** bit (LCR[7]) is set and the UART is not busy (**UART Busy** = 0). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor) Note that with the Divisor Latch Registers (**DLL** and **DLH**) set to zero, the baud clock is disabled and no serial communications occur. Also, once the **DLL** is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

9.3.5.4. UART Divisor Latch High Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: UART_DLH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register contains the baud rate divisor for the UART. This register may only be accessed when the **DLAB** bit (LCR[7]) is set and the UART is not busy (**UART Busy** = 0). The output baud rate is equal to the serial clock (sclk) frequency divided by

			sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor) Note that with the Divisor Latch Registers (**DLL** and **DLH**) set to zero, the baud clock is disabled and no serial communications occur. Also, once the **DLH** is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

9.3.5.5. UART Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: UART_IER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:4	/	/	/
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available

			Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

9.3.5.6. UART Interrupt Identity Register(Default Value: 0x0000_0001)

Offset: 0x0008			**Register Name: UART_IIR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset**
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)

			FIFOs enabled)	
1100	Second	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Third	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Fifth	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

9.3.5.7. UART FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: UART_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated

			when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 1: Mode 1
2	W	0x0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

9.3.5.8. UART Line Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: UART_LCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writable only when UART is not busy (**UART Busy** = 0) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (**UART_DLL** and **UART_DLH**) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (**UART_RBR**) / TX Holding Register(**UART_THR**) and Interrupt Enable Register (**UART_IER**) 1: Select Divisor Latch Low Register (**UART_DLL**) and Divisor Latch High

			Register (**UART_DLH**)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in **Loop Back Mode**, as determined by **UART_MCR[4]**, the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (**UART_MCR[6]** is set to 1) the sir_out_n line is continuously pulsed. When in **Loop Back Mode**, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0x0	EPS Even Parity Select It is writable only when UART is not busy (**UART Busy** = 0) .This is used to select even and odd parity when parity is enabled (**PEN** is set to one). Setting the bit5 is to reverse the bit4. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4]
3	R/W	0x0	PEN Parity Enable It is writable only when UART is not busy (**UART Busy** = 0) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: Parity disabled 1: Parity enabled
2	R/W	0x0	STOP Number of stop bits It is writable only when UART is not busy (**UART Busy** = 0) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If the bit is set to zero, one stop bit is transmitted in the serial data. If the bit is set to one and the **Data Length** are set to 5 bits (**DLS** =0) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when **DLS** is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writable only when UART is not busy (**UART Busy** = 0) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected is as follows:

			00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

9.3.5.9. UART Modem Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	SIRE SIR Mode Enable 0: IrDA SIR mode disable 1: IrDA SIR mode enable
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (**AFCE**) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disable 1: Auto Flow Control Mode enable
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, **UART_MCR[6]** is set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in **Loop Back Mode**, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, **UART_MCR[6]** set to 1), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that

			the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (**AFCE** = 0), the rts_n signal is set low by programming **RTS** to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (**AFCE** = 1) and FIFOs enable (**FIFOE** =1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when **RTS** is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (**LOOP** =1), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the **DTR** (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (**LOOP** =1), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

9.3.5.10. UART Line Status Register(Default Value: 0x0000_0060)

Offset: 0x0014			**Register Name: UART_LSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the **UART_LSR** register provided there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the *TX Holding Register* and the *TX Shift Register* are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the *TX Shift Register* are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE

			TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the *TX Holding Register* is empty and ready to accept new data and it is cleared when the CPU writes to the *TX Holding Register*. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. In UART mode (**SIRE** = 0), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of ***start time + data bits + parity + stop bits***. In infrared mode (**SIRE** = 1), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of ***start time + data bits + parity + stop bits***. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the **BI** bit. In the non-FIFO mode, the **BI** indication occurs immediately and persists until the LSR is read.
3	R	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the **FE** bit is set if a break interrupt has occurred, as indicated by the **BI** bit. 0: No framing error 1: Framing error Reading the LSR clears the **FE** bit.
2	R	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the **PEN** bit is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the **PE** bit is set if a break interrupt has occurred, as indicated by the **Break Interrupt** bit.

			0: No parity error 1: Parity error Reading the LSR clears the **PE** bit.
1	R	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the **OE** bit is set when a new character arrives in the receiver before the previous character was read from the **Receiver Buffer Register**. When this happens, the data in the **Receiver Buffer Register** is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: No overrun error 1: Overrun error Reading the LSR clears the **OE** bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the **Receiver Buffer Register** or the receiver FIFO. 0: No data ready 1: Data ready This bit is cleared when the **Receiver Buffer Register** is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

9.3.5.11. UART Modem Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			**Register Name: UART_MSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the **Data Carrier Detect** input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)

6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the **Ring Indicator** input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the **Data Set Ready** input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In **Loop Back Mode** (MCR[4] set to one), **DSR** is the same as MCR[0] (**DTR**).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the **Clear To Send** input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In **Loop Back Mode** (MCR[4] = 1), CTS is the same as MCR[1] (**RTS**).
3	R	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the **DDCD** bit. **Note:** If the **DDCD** bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	R	0x0	TERI Trailing Edge Ring Indicator

			This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the **DDSR** bit. In **Loop Back Mode** (MCR[4] = 1), DDSR reflects changes on MCR[0] (**DTR**). **Note:** If the **DDSR** bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the **DDSR** bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the **DCTS** bit. In **Loop Back Mode** (MCR[4] = 1), DCTS reflects changes on MCR[1] (**RTS**). **Note:** If the **DCTS** bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the **DCTS** bit is set when the reset is removed if the cts_n signal remains asserted.

9.3.5.12. UART Scratch Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: UART_SCH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

9.3.5.13. UART Status Register(Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

9.3.5.14. UART Transmit FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

9.3.5.15. UART Receive FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

9.3.5.16. UART Halt TX Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/W	0x0	CHANGE_UPDATE After the user use HALT[1] to change the baud rate or **UART_LCR** configuration. Write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Writing 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY

			This is an enable bit for the user to change **UART_LCR** register configuration (except for the **DLAB** bit) and baud rate register (**DLL** and **DLH**) when the UART is busy. 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled **Note:** If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

9.4. CIR Receiver

9.4.1. Overview

The CIR (Consumer infrared) Receiver module receives data over the IR interface.

Features:

- Full physical layer implementation
- Supports IR for remote control
- 64x8 bits FIFO for data buffer
- Programmable FIFO thresholds

For saving CPU resource, CIR receiver is implemented in hardware. The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' and the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

In the air, there is always some noise. One threshold can be set to filter the noise to reduce system loading and improve the system stability.

9.4.2. Register List

Module Name	Base Address
CIR	0x01F02000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Control Register
CIR_RXCTL	0x0010	CIR Receiver Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_CONFIG	0x0034	CIR Configure Register

9.4.3. Register Description

9.4.3.1. CIR Receiver Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	CGPO General Program Output (GPO) Control in CIR mode for TX Pin 0: Low level 1: High level
7:6	/	/	/
5:4	R/W	0x0	CIR_ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

9.4.3.2. CIR Receiver Configure Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

9.4.3.3. CIR Receiver FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	Receiver Byte FIFO

9.4.3.4. CIR Receiver Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching **RAL**. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching **RAL**. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

9.4.3.5. CIR Receiver Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:8	R	0x0	RAC RX FIFO Available Counter 0000000: No available data in RX FIFO 0000001: 1 byte available data in RX FIFO 0000010: 2 byte available data in RX FIFO … 1000000: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0: Idle 1: Busy
6:5	/	/	/
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: One CIR symbol is receiving or not detected. 1: One CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W1C	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

9.4.3.6. CIR Receiver Configure Register(Default Value: 0x0000_1828)

Offset: 0x0034			Register Name: CIR_RCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0: ATHR in Unit of (Sample Clock) 1: ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses the field to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver retains in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU. When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.
7:2	R/W	0xa	NTHR Noise Threshold for CIR When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware. 000000: All samples are recorded into RX FIFO 000001: If the signal is only one sample duration, it is taken as noise and discarded. 000010: If the signal is less than (<=) two sample duration, it is taken as noise and discarded. … 111101: If the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.
1:0	R/W	0x0	SCS

Sample Clock Select for CIR

SCS2	SCS[1]	SCS[0]	Sample Clock
0	0	0	ir_clk/64
0	0	1	ir_clk/128
0	1	0	ir_clk/256
0	1	1	ir_clk/512
1	0	0	ir_clk
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

9.5. USB

9.5.1. USB OTG Controller

9.5.1.1. Overview

The USB OTG is a Dual-Role Device controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

Features:

- Complies with USB 2.0 Specification
- Supports Device or Host operation at a time
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in host mode
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in device mode
- Supports bi-directional endpoint0 for Control transfer in device mode
- Supports up to 8 User-Configurable Endpoints for Bulk,Isochronousl and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4) in device mode
- Supports up to (4KB+64B) FIFO for EPs (Excluding EP0) in device mode
- Supports the UTMI+ Level 3 interface . The 8-bit bidirectional data buses are used
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Power Optimization and Power Management capabilities

9.5.1.2. Block Diagram

Figure 9-7 shows the block diagram of USB OTG Controller.

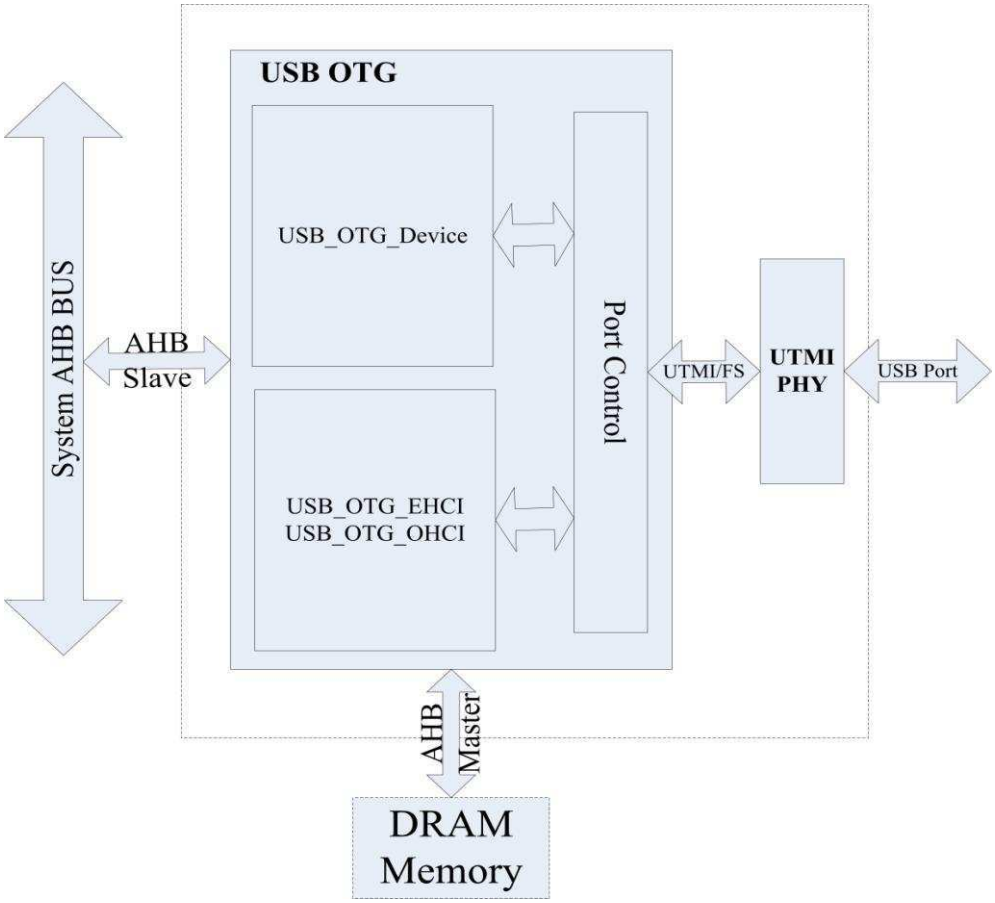


Figure 9-7. USB OTG Controller Block Diagram

9.5.2. USB Host Controller

9.5.2.1. Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

Features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Supports 32-bit Little Endian AMBA AHB Slave Bus for Register Access.
- Supports 32-bit Little Endian AMBA AHB Master Bus for Memory Access.
- Including an internal DMA Controller for data transfer with memory.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Supports the UTMI+ Level 3 interface . The 8-bit bidirectional data buses are used.

- Supports only 1 USB Root Port shared between EHCI and OHCI.

9.5.2.2. Block Diagram

Figure 9-8 shows the USB Host Controller system-level block diagram.

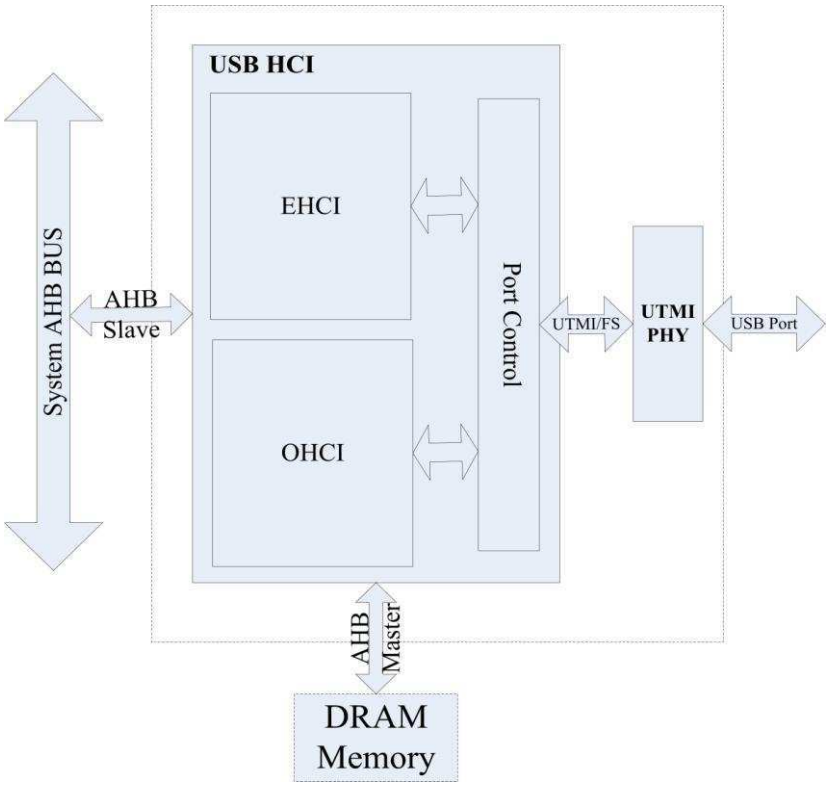


Figure 9-8. USB Host Controller Block Diagram

9.5.2.3. USB Host Timing Diagram

Please refer USB2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

9.5.2.4. USB Host Register List

Module Name	Base Address
USB_HCI1	0x01C1B000
USB_HCI2	0x01C1C000
USB_HCI3	0x01C1D000

Register Name	Offset	Description
EHCI Capability Register		

E_CAPLENGTH	0x000	EHCI Capability Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x00C	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x400	OHCI Revision Register
O_HcControl	0x404	OHCI Control Register
O_HcCommandStatus	0x408	OHCI Command Status Register
O_HcInterruptStatus	0x40C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x418	OHCI HCCA Base
O_HcPeriodCurrentED	0x41c	OHCI Period Current ED Base
O_HcControlHeadED	0x420	OHCI Control Head ED Base
O_HcControlCurrentED	0x424	OHCI Control Current ED Base
O_HcBulkHeadED	0x428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x42C	OHCI Bulk Current ED Base
O_HcDoneHead	0x430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x434	OHCI Frame Interval Register
O_HcFmRemaining	0x438	OHCI Frame Remaining Register
O_HcFmNumber	0x43C	OHCI Frame Number Register
O_HcPerioddicStart	0x440	OHCI Periodic Start Register
O_HcLSThreshold	0x444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x44C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x454	OHCI Root Hub Port Status Register

9.5.2.5. EHCI Register Description

9.5.2.5.1. EHCI Capability Length Register(Default Value: Implementation Dependent)

Offset: 0x0000			Register Name: CAPLENGTH
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

9.5.2.5.2. EHCI Host Interface Version Number Register(Default Value: 0x0100)

Offset: 0x0002			Register Name: HCIVERSION
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R	0x0100	HCIVERSION This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

9.5.2.5.3. EHCI Host Control Structural Parameter Register(Default Value: Implementation Dependent)

Offset: 0x0004			Register Name: HCSPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	0x0	Reserved. These bits are reserved and should be set to zero.
23:20	R	0x0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	0x0	Reserved. These bits are reserved and should be set to zero.
15:12	R	0x0	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0x0	Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software.

<table>
<tr><td></td><td></td><td></td><td>This field will always fix with ‘0’.</td></tr>
<tr><td>7</td><td>R</td><td>0x0</td><td>Port Routing Rules
This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation:
<table><tr><td>Value</td><td>Meaning</td></tr><tr><td>0</td><td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td></tr><tr><td>1</td><td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td></tr></table>This field will always be ‘0’.</td></tr>
<tr><td>6:4</td><td>/</td><td>0x0</td><td>Reserved.
These bits are reserved and should be set to zero.</td></tr>
<tr><td>3:0</td><td>R</td><td>0x1</td><td>N_PORTS
This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f.
This field is always 1.</td></tr>
</table>

9.5.2.5.4. EHCI Host Control Capability Parameter Register(Default Value: Implementation Dependent)

Offset: 0x0008			**Register Name: HCCPARAMS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	0x0	Reserved These bits are reserved and should be set to zero.
15:18	R	0x0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always ‘00b’.
7:4	R	0x0	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.

3	R	0x0	Reserved These bits are reserved and should be set to zero.
2	R	0x0	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	0x0	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.
0	R	0x0	Reserved These bits are reserved for future use and should return a value of zero when read.

9.5.2.5.5. EHCI Companion Port Route Description(Default Value: UDF)

Offset: 0x000C			**Register Name: HCSP-PORTROUTE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	UDF	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

9.5.2.5.6. EHCI USB Command Register(Default Value: 0x0008_0000)

The default value is 0x00080B00 if Asynchronous Schedule Park Capability is a one.

<table>
<tr><td colspan="3">Offset: 0x0010</td><td>Register Name: USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:24</td><td>/</td><td>0x0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x8</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table>
<tr><td>Value</td><td>Minimum Interrupt Interval</td></tr>
<tr><td>0x00</td><td>Reserved</td></tr>
<tr><td>0x01</td><td>1 micro-frame</td></tr>
<tr><td>0x02</td><td>2 micro-frame</td></tr>
<tr><td>0x04</td><td>4 micro-frame</td></tr>
<tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr>
<tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr>
<tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr>
<tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr>
</table>
Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>0x0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>11</td><td>R/W or R</td><td>0x0</td><td>Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>0x0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>9:8</td><td>R/W or R</td><td>0x0</td><td>Asynchronous Schedule Park Mode Count(OPTIONAL)
Asynchronous Park Capability bit in the HCCPARAMS register is a one.Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.
Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Light Host Controller Reset(OPTIONAL)
This control bit is not required.
If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>default values and the CF bit setting should not go to zero (retaining port ownership relationships).
A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-
Ware must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W or R</td><td>0x0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:
<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096bytes)Default</td></tr><tr><td>01b</td><td>512 elements(2048byts)</td></tr><tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
</table>

1	R/W	0x0	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0x0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

9.5.2.5.7. EHCI USB Status Register(Default Value: 0x0000_1000)

Offset: 0x0014			**Register Name: USBSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	0x0	Reserved These bits are reserved and should be set to zero.
15	R	0x0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).

14	R	0x0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	0x0	Reserved These bits are reserved and should be set to zero.
5	R/WC	0x0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0x0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	USB Error Interrupt(USBERRINT)

			The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

9.5.2.5.8. EHCI USB Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0018			**Register Name: USBINTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	0x0	Reserved These bits are reserved and should be zero.
5	R/W	0x0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

9.5.2.5.9. EHCI Frame Index Register (Default Value: 0x0000_0000)

<table>
<tr><td colspan="3">Offset: 0x001C</td><td>Register Name: FRINDEX</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:14</td><td>/</td><td>0x0</td><td>Reserved
These bits are reserved and should be zero.</td></tr>
<tr><td>13:0</td><td>R/W</td><td>0x0</td><td>Frame Index
The value in this register increment at the end of each time frame (e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It Means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.
<table>
<tr><td>USBCMD[Frame List Size]</td><td>Number Elements</td><td>N</td></tr>
<tr><td>00b</td><td>1024</td><td>12</td></tr>
<tr><td>01b</td><td>512</td><td>11</td></tr>
<tr><td>10b</td><td>256</td><td>10</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td></tr>
</table></td></tr>
</table>

Note: This register must be written as a DWord. Byte writes produce undefined results.

9.5.2.5.10. EHCI Periodic Frame List Base Address Register (Default Value: UDF)

Offset: 0x0024			**Register Name: PERIODICLISTBASE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	UDF	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	UDF	Reserved Must be written as 0x0 during runtime, the values of these bits are undefined.

Note: Writes must be Dword Writes.

9.5.2.5.11. EHCI Current Asynchronous List Address Register (Default Value: UDF)

Offset: 0x0028			Register Name: ASYNCLISTADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	R/W	UDF	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	0x0	Reserved These bits are reserved and their value has no effect on operation. Bits in this field cannot be modified by system software and will always return a zero when read.

Note: Write must be DWord Writes.

9.5.2.5.12. EHCI Configure Flag Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CONFIGFLAG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	0x0	Reserved These bits are reserved and should be set to zero.
0	R/W	0x0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 – Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 – Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

Note: This register is not used in the normal implementation.

9.5.2.5.13. EHCI Port Status and Control Register(Default Value: 0x0000_2000(w/PPC set to one))

The default value is 0x00003000 when w/PPC set to a zero.

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	0x0	Reserved These bits are reserved for future use and should return a value of zero when

<table>
<tr><td></td><td></td><td></td><td>read.</td></tr>
<tr><td>21</td><td>R/W</td><td>0x0</td><td>Wake on Disconnect Enable(WKDSCNNT_E)
Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>20</td><td>R/W</td><td>0x0</td><td>Wake on Connect Enable(WKCNNT_E)
Writing this bit to a one enable the port to be sensitive to device connects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0x0</td><td>Port Test Control
The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow:
<table>
<tr><td>Bits</td><td>Test Mode</td></tr>
<tr><td>0000b</td><td>The port is NOT operating in a test mode.</td></tr>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-1111b</td><td>Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.</td></tr>
<tr><td>15:14</td><td>R/W</td><td>0x0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>13</td><td>R/W</td><td>0x1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>0x0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>11:10</td><td>R</td><td>0x0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>0x0</td><td>Reserved
This bit is reserved for future use, and should return a value of zero when read.</td></tr>
<tr><td>8</td><td>R/W</td><td>0x0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit.
Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table>
<tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr>
<tr><td>0x</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
<tr><td>11</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current</td></tr>
</table>

			transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: ① Software sets the Force Port Resume bit to a zero(from a one). ② Software sets the Port Reset bit to a one(from a zero). If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'.
6	R/W	0x0	Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0x0	Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0x0	Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change.

			For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0x0	Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

Note: This register is only reset by hardware or in response to a host controller reset.

9.5.2.6. OHCI Register Description

9.5.2.6.1. HcRevision Register(Default Value: 0x0000_0010)

Offset: 0x400				**Register Name: HcRevision**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:8	/	/	0x00	Reserved

7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

9.5.2.6.2. HcControl Register(Default Value: 0x0000_0000)

Offset: 0x404				**Register Name: HcRevision**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:11	/	/	0x00	Reserved
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
8	R/W	R	0x0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	R/W	0x0	HostControllerFunctionalState for USB 00b USBReset 01b USBResume 10b USBOperational 11b USBSuspend A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after

<table>
<tr><td></td><td></td><td></td><td></td><td>detecting the resume signaling from a downstream port.
HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.</td></tr>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>BulkListEnable
This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>4</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlListEnable
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>3</td><td>R/W</td><td>R</td><td>0x0</td><td>IsochronousEnable
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.
Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).</td></tr>
<tr><td>2</td><td>R/W</td><td>R</td><td>0x0</td><td>PeriodicListEnable
This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlBulkServiceRatio
This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
<table>
<tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr>
<tr><td>0</td><td>1:1</td></tr>
<tr><td>1</td><td>2:1</td></tr>
<tr><td>2</td><td>3:1</td></tr>
<tr><td>3</td><td>4:1</td></tr>
</table>
The default value is 0x0.</td></tr>
</table>

9.5.2.6.3. HcCommandStatus Register(Default Value: 0x0000_0000)

Offset: 0x408				Register Name: HcCommandStatus
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	0x0	Reserved
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the

				InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

9.5.2.6.4. HcInterruptStatus Register(Default Value: 0x0000_0000)

Offset: 0x40C				**Register Name: HcInterruptStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:7	/	/	0x0	Reserved
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

9.5.2.6.5. HcInterruptEnable Register(Default Value: 0x0000_0000)

Offset: 0x410				Register Name: HcInterruptEnable Register
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	0x0	Reserved
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

9.5.2.6.6. HcInterruptDisable Register(Default Value: 0x0000_0000)

Offset: 0x414				Register Name: HcInterruptDisable Register
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	0x00	Reserved

6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Write back Done Head;
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Scheduling Overrun;

9.5.2.6.7. HcHCCA Register(Default Value: 0x0000_0000)

Offset: 0x418				**Register Name: HcHCCA**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

9.5.2.6.8. HcPeriodCurrentED Register(Default Value: 0x0000_0000)

Offset: 0x41C				**Register Name: HcPeriodCurrentED(PCED)**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		

31:4	R	R/W	0x0	PCED[31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

9.5.2.6.9. HcControlHeadED Register(Default Value: 0x0000_0000)

Offset: 0x420				**Register Name: HcControlHeadED[CHED]**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R/W	R	0x0	EHCD[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

9.5.2.6.10. HcControlCurrentED Register(Default Value: 0x0000_0000)

Offset: 0x424				**Register Name: HcControlCurrentED[CCED]**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.

3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

9.5.2.6.11. HcBulkHeadED Register(Default Value: 0x0000_0000)

Offset: 0x428				**Register Name: HcBulkHeadED[BHED]**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R/W	R	0x0	BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

9.5.2.6.12. HcBulkCurrentED Register(Default Value: 0x0000_0000)

Offset: 0x42C				**Register Name: HcBulkCurrentED [BCED]**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:4	R/W	R/W	0x0	BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

9.5.2.6.13. HcDoneHead Register(Default Value: 0x0000_0000)

Offset: 0x430				Register Name: HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0	R	R	0x0	HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

9.5.2.6.14. HcFmInterval Register(Default Value: 0x0000_2EDF)

Offset: 0x434				Register Name: HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	0x0	Reserved
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

9.5.2.6.15. HcFmRemaining Register(Default Value: 0x0000_0000)

Offset: 0x438			Register Name: HcFmRemaining
Bit	Read/Write	Default/Hex	Description

	HCD	HC		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	0x0	Reserved
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

9.5.2.6.16. HcFmNumber Register(Default Value: 0x0000_0000)

Offset: 0x43c				Register Name: HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	0x0	Reserved
15:0	R	R/W	0x0	FrameNumber This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

9.5.2.6.17. HcPeriodicStart Register(Default Value: 0x0000_0000)

Offset: 0x440				Register Name: HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	0x0	Reserved
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 0x2A3F (0x3e67). When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

9.5.2.6.18. HcLSThreshold Register(Default Value: 0x0000_0628)

Offset: 0x444				Register Name: HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	0x0	Reserved
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

9.5.2.6.19. HcRhDescriptorA Register(Default Value: 0x0200_1201)

Offset: 0x448				Register Name: HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	0x0	Reserved
12	R/W	R	0x1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 Over-current status is reported collectively for all downstream ports. 1 No overcurrent protection supported.
11	R/W	R	0x0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 Over-current status is reported collectively for all downstream ports. 1 Over-current status is reported on per-port basis.
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	0x1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports

				is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0 – All ports are powered at the same time. 1 – Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
8	R/W	R	0x0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 – Ports are power switched. 1 – Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

9.5.2.6.20. HcRhDescriptorB Register(Default Value: 0x0000_0000)

Offset: 0x44C				**Register Name: HcRhDescriptorB Register**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 – Reserved Bit1 – Ganged-power mask on Port #1. Bit2 – Ganged-power mask on Port #2. … Bit15 – Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable.

				Bit0	Reserved
				Bit1	Device attached to Port #1.
				Bit2	Device attached to Port #2.
				…	
				Bit15	Device attached to Port #15.

9.5.2.6.21. HcRhStatus Register(Default Value: 0x0000_0000)

Offset: 0x450				Register Name: HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	(write)ClearRemoteWakeupEnable Write a ‘1’ clears DeviceRemoteWakeupEnable. Write a ‘0’ has no effect.
30:18	/	/	0x0	Reserved
17	R/W	R	0x0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a ‘1’. Writing a ‘0’ has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 – ConnectStatusChange is not a remote wakeup event. 1 – ConnectStatusChange is a remote wakeup event. (write)SetRemoteWakeupEnable Writing a ‘1’ sets DeviceRemoveWakeupEnable. Writing a ‘0’ has no effect.
14:2				Reserved
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always ‘0’
0	R/W	R	0x0	(Read)LocalPowerStatus

				When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

9.5.2.6.22. HcRhPortStatus Register(Default Value: 0x0000_0100)

Offset: 0x454				**Register Name: HcRhPortStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not completed 1 port reset is completed
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortEnableStatus 1 change in PortEnableStatus
16	R/W	R/W	0x0	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD

<table>
<tr><td></td><td></td><td></td><td></td><td>writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.
<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>
Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>-</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.
<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.

Note: This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
</table>

<table>
<tr><td>7:5</td><td>/</td><td>/</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>
(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event,</td></tr>
</table>

				switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 port is disabled 1 port is enabled (write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0 No device connected 1 Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read '1' when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).

9.5.2.7. HCI Interface Control and Status Register Description

9.5.2.7.1. HCI Interface Control Register(Default Value: 0x0000_0000)

Offset: 0x800			Register Name: HCI_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	Reserved.
20	R/W	0x0	EHCI HS force Set 1 to this field force the ehci enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19:18	/	/	/
17	R/W	0x0	HSIC Connect detect 1 in this field enable the hsic phy to detect device connect pulse on the bus. This field only valid when the bit 1 is set.
16	R/W	0x0	HSIC Connect Interrupt Enable Enable the HSIC connect interrupt. This field only valid when the bit 1 is set.
15:13	/	/	/

12	/	/	/
11	R/W	0x0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: Do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0x0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: do not use INCR8,use other enabled INCRX or unspecified length burst INCR
9	R/W	0x0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: do not use INCR4,use other enabled INCRX or unspecified length burst INCR
8	R/W	0x0	AHB Master interface INCRX align enable 1: Start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of 11:9 is enabled
7:2	/	/	Reserved
1	R/W	0x0	HSIC 0:/ 1:HSIC This meaning is only valid when the controller is HCI1.
0	R/W	0x0	ULPI bypass enable 1: Enable UTMI interface, disable ULPI interface(SP used utmi interface) 0: Enable ULPI interface, disable UTMI interface

9.5.2.7.2. HSIC status Register(Default Value: 0x0000_0000)

Offset: 0x804			**Register Name: HSIC_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSIC Connect Status 1 in this field indicates a device connect pulse being detected on the bus. This field only valid when the EHCI HS force bit and the HSIC Phy Select bit is set. When the HSIC Connect Interrupt Enable is set, 1 in this bit will generate an interrupt to the system. This register is valid on HCI1.
15:0	/	/	/

9.5.2.8. USB Host Clock Requirement

Name	Description
HCLK	System clock (provided by AHB bus clock). This clock needs to be >30MHz.
CLK60M	Clock from PHY for HS SIE, is constant to be 60MHz.
CLK48M	Clock from PLL for FS/LS SIE, is constant to be 48MHz.

9.6. SCR

9.6.1. Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation. cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

Features:

- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

9.6.2. Block Diagram

The top diagram of Smart Card Reader is below.

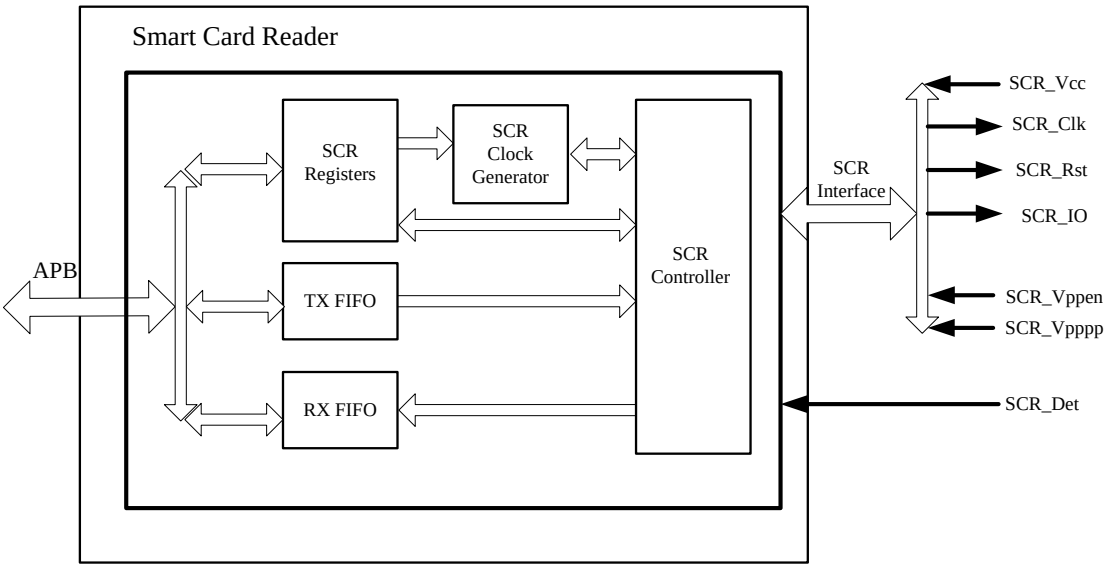


Figure 9-9. SCR Block Diagram

9.6.3. Operations and Functional Descriptions

9.6.3.1. External Signals

The following table describes the external signals of SCR.

Table 9-9. SCR External Signals

Pin Name	Description	Type
SIM0_PWREN	Smart Card 0 Power Enable	O
SIM0_CLK	Smart Card 0 Clock	O
SIM0_DATA	Smart Card 0 Data	I/O
SIM0_RST	Smart Card 0 Reset	O
SIM0_DET	Smart Card 0 Detect	I
SIM0_VPPEN	Smart Card 0 Program Voltage Enable	O
SIM0_VPPPP	Smart Card 0 Program Control	O
SIM1_PWREN	Smart Card 1 Power Enable	O
SIM1_CLK	Smart Card 1 Clock	O
SIM1_DATA	Smart Card 1 Data	I/O
SIM1_RST	Smart Card 1 Reset	O
SIM1_DET	Smart Card 1 Detect	I
SIM1_VPPEN	Smart Card 1 Program Voltage Enable	O
SIM1_VPPPP	Smart Card 1 Program Control	O

9.6.3.2. SCR Timing Diagram

Please refer ISO/IEC 7816 and EMV2000 Specification.

9.6.3.3. Clock Generator

The Clock Generator generates the SCR clock signal and the Baud Clock Impulse signal, used in the timing of SCR.

The SCR clock signal is used as the main clock for the Smart Card. Its frequency can be adjusted using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock. The SCCLK frequency is given by the following equation:

$$f_{scclk} = \frac{f_{sysclk}}{2 * (SCCDIV + 1)}$$

f_{scclk} -- Smart Card Clock Frequency

f_{sysclk} -- System Clock (PCLK) Frequency

The Baud Clock Impulse signal is used to transmit and receive serial between the SCR and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV). The value is used to divide the system clock. The BUAD rate is given by the following equation:

$$BAUD = \frac{f_{sysclk}}{2 * (BAUDDIV + 1)}$$

$BAUD$ -- Baud rate of the data stream between Smart Card and Reader.

The duration of one bit, Elementary Time Unit (ETU), is defined in the ISO/IEC 7816-3 specification. During the first answer to reset response after the cold reset, the initial ETU must be equal to 372 Smart Card Clock Cycles.

$$\frac{1}{BAUD} = ETU = \frac{372}{f_{scclk}}$$

In this case, the BAUDDIV should be

$$BAUDDIV = \frac{372 * f_{sysclk}}{2 * f_{scclk}} - 1 = 372 * (SCCDIV + 1) - 1 .$$

After the ATR is completed, the ETU can be changed according to Smart Card abilities.

$$\frac{1}{BAUD} = ETU = \frac{F}{D} * \frac{1}{f_{scclk}}$$

Parameters F and D are defined in the ISO/IEC 7816-3 Specification.

9.6.3.4. SCIO Pad Configuration

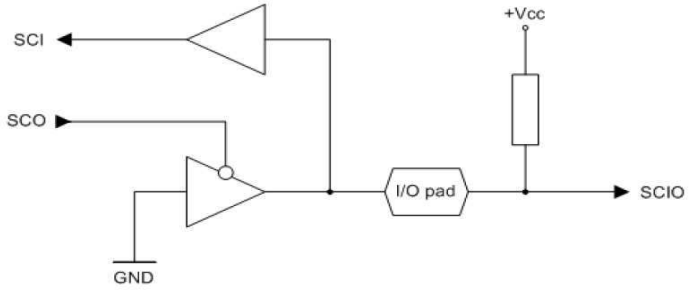


Figure 9-10. SCIO Pad Configuration Diagram

9.6.4. Register List

Module Name	Base Address
SCR0	0x01C2C400
SCR1	0x01C2C800

Register Name	Offset	Description
SCR_CSR	0x0000	Smart Card Reader Control and Status Register
SCR_INTEN	0x0004	Smart Card Reader Interrupt Enable Register 1
SCR_INTST	0x0008	Smart Card Reader Interrupt Status Register 1
SCR_FCSR	0x000C	Smart Card Reader FIFO Control and Status Register
SCR_FCNT	0x0010	Smart Card Reader RX and TX FIFO Counter Register
SCR_RPT	0x0014	Smart Card Reader RX and TX Repeat Register
SCR_DIV	0x0018	Smart Card Reader Clock and Baud Divisor Register
SCR_LTIM	0x001C	Smart Card Reader Line Time Register
SCR_CTIM	0x0020	Smart Card Reader Character Time Register
SCR_LCTLR	0x0030	Smart Card Reader Line Control Register
SCR_FIFO	0x0100	Smart Card Reader RX and TX FIFO Access Point

9.6.5. Register Description

9.6.5.1. Smart Card Reader Control and Status Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: SCR_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	SCDET Smart Card Detected This bit is set to '1' when the scdetect input is active at least for a debounce time.
30	/	/	/
24	R/W	0x0	SCDETPOL Smart Card Detect Polarity This bit set polarity of scdetect signal. 0: Low Active 1: High Active
23:22	R/W	0x0	Protocol Selection (PTLSEL) 00: T=0. 01: T=1, no character repeating and no guard time is used when T=1 protocol is selected. 10: Reserved 11: Reserved
21	R/W	0x0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
20	R/W	0x0	TSRXE TS Receive Enable When set to '1', the TS character (the first ATR character) will be stored in RXFIFO during card session.
19	R/W	0x0	CLKSTPPOL Clock Stop Polarity The value of the scclk output during the clock stop state.
18	R/W	0x0	PECRXE Parity Error Character Receive Enable Enables storage of the characters received with wrong parity in RX FIFO.
17	R/W	0x0	MSBF MSB First When high, inverse bit ordering convention (msb to lsb) is used.
16	R/W	0x0	DATAPOL Data Plorarity When high, inverse level convention is used (A='1', Z='0').
15:12	/	/	/

11	R/W	0x0	DEACT Deactivation. Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the **DEACT** bit is automatically cleared.
10	R/W	0x0	ACT Activation. Setting of this bit initializes the activation sequence. When the activation is finished, the **ACT** bit is automatically cleared.
9	R/W	0x0	WARMRST Warm Reset Command. Writing '1' to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
8	R/W	0x0	CLKSTOP Clock Stop. When this bit is asserted and the Smart Card I/O line is in 'Z' state, the SCR core stops driving of the Smart Card clock signal after the CLKSTOPDELAY time expires. The Smart Card clock is restarted immediately after the **CLKSTOP** signal is deasserted. New character transmission can be started after CLKSTARTDELAY time. The expiration of both times is signaled by the CLKSTOPRUN bit in the interrupt registers.
7:3	/	/	Reserved
2	R/W	0x0	GINTEN Global Interrupt Enable. When high, IRQ output assertion is enabled.
1	R/W	0x0	RXEN Receiving Enable. When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
0	R/W	0x0	TXEN Transmission Enable. When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card.

9.6.5.2. Smart Card Reader Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: SCR_INTEN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt Enable.
22	R/W	0x0	SCACT Smart Card Activation Interrupt Enable.
21	R/W	0x0	SCINS

			Smart Card Inserted Interrupt Enable.
20	R/W	0x0	SCREM Smart Card Removed Interrupt Enable.
19	R/W	0x0	ATRDONE ATR Done Interrupt Enable.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt Enable.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt Enable.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt Enable.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt Enable.
11	R/W	0x0	RXDONE RX Done Interrupt Enable.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt Enable.
9	R/W	0x0	RXFIFOFULL RX FIFO Full Interrupt Enable.
8	/	/	/
7:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt Enable.
3	R/W	0x0	TXDONE TX Done Interrupt Enable.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt Enable.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt Enable.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt Enable.

9.6.5.3. Smart Card Reader Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: SCR_INTST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt. When enabled, this interrupt is asserted after the Smart Card deactivation sequence completed.
22	R/W	0x0	SCACT Smart Card Activation Interrupt.

			When enabled, this interrupt is asserted after the Smart Card activation sequence completed.
21	R/W	0x0	SCINS Smart Card Inserted Interrupt. When enabled, this interrupt is asserted after the Smart Card inserted.
20	R/W	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the Smart Card removed.
19	R/W	0x0	ATRDONE ATR Done Interrupt. When enabled, this interrupt is asserted after the ATR sequence successfully completed.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt. When enabled, this interrupt is asserted if the ATR sequence fails.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt. When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt. When enabled, this interrupt is asserted in two cases: ● When the Smart Card clock is stopped. ● When the new character can be started after the clock restart. To distinguish between the two interrupt cases, we recommend reading the **CLKSTOP** bit in SCR_CSR register.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt. When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used.
11	R/W	0x0	RXDONE RX Done Interrupt. When enabled, this interrupt is asserted after a character was received from the Smart Card.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
9	R/W	0x0	RXFIFOFULL

			RX FIFO Full Interrupt. When enabled, this interrupt is asserted if the RX FIFO is filled up.
8	/	/	/
7:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard time after the character transmission was repeated TXREPEAT times or T=1 protocol is used.
3	R/W	0x0	TXDONE TX Done Interrupt. When enabled, this interrupt is asserted after one character was transmitted to the Smart Card.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt. When enabled, this interrupt is asserted after all bytes from TX FIFO are transferred to the Smart Card.

Note: This register provides information about the state of each interrupt bit. You can clear the register bits individually by writing '1' to a bit you intend to clear.

9.6.5.4. Smart Card Reader FIFO Control and Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: SCR_FCSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	RXFIFOFLUSH Flush RX FIFO. RX FIFO is flushed, when '1' is written to this bit.
9	R	0x0	RXFIFOFULL RX FIFO Full.
8	R	0x1	RXFIFOEMPTY RX FIFO Empty.
7:3	/	/	/
2	R/W	0x0	TXFIFOFLUSH Flush TX FIFO. TX FIFO is flushed, when '1' is written to this bit.
1	R	0x0	TXFIFOFULL TX FIFO Full.
0	R	0x1	TXFIFOEMPTY

			TX FIFO Empty.

9.6.5.5. Smart Card Reader FIFO Counter Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SCR_FIFOCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	RXFTH RX FIFO Threshold These bits set the interrupt threshold of RX FIFO. The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold.
23:16	R/W	0x0	TXFTH TX FIFO Threshold These bits set the interrupt threshold of TX FIFO. The interrupt is asserted when the number of bytes in TX FIFO is equal to or less than the threshold.
15:8	R	0x0	RXFCNT RX FIFO Counter These bits provide the number of bytes stored in the RXFIFO.
7:0	R	0x0	TXFCNT TX FIFO Counter These bits provide the number of bytes stored in the TXFIFO.

9.6.5.6. Smart Card Reader Repeat Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: SCR_REPEAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	RXRPT RX Repeat This is a 4-bit register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the error signal during the guard time.
3:0	R/W	0x0	TXRPT TX Repeat This is a 4-bit register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guard time.

9.6.5.7. Smart Card Reader Clock Divisor Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SCR_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0x0	BAUDDIV Baud Clock Divisor. This 16-bit register defines the divisor value used to generate the Baud Clock impulses from the system clock. $BAUD = \frac{f_{sysclk}}{2 * (BAUDDIV + 1)}$
15:0	R/W	0x0	SCCDIV Smart Card Clock Divisor. This 16-bit register defines the divisor value used to generate the Smart Card Clock from the system clock. $f_{scclk} = \frac{f_{sysclk}}{2 * (SCCDIV + 1)}$ f_{scclk} is the frequency of Smart Card Clock Signal. f_{sysclk} is the frequency of APB Clock.

9.6.5.8. Smart Card Reader Line Time Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SCR_LTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	ATR ATR Start Limit. This 16-bit register defines the maximum time between the rising edge of the scrstn signal and the start of ATR response. ATR Start Limit = 128* ATR*T_{scclk}
15:8	R/W	0x0	RST Reset Duration. This 16-bit register sets the duration of the Smart Card reset sequence. This value is same for the cold and warm reset. Cold/Warm Reset Duration = 128* RST* T_{scclk}
7:0	R/W	0x0	ACT Activation/Deactivation Time. This 16-bit register sets the duration of each part of the activation and deactivation sequence. Activation/Deactivation Duration = 128* ACT * T_{scclk} $T_{scclk} = \frac{1}{f_{scclk}}$ is the Smart Card Clock Cycle.

9.6.5.9. Smart Card Reader Character Time Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: **SCR_CTIM**
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CHARLIMIT Character Limit. This 16-bit register sets the maximum time between the leading edges of two consecutive characters. The value is ETUs.
15:8	/	/	/
7:0	R/W	0x0	GUARDTIME Character Guard time. This 8-bit register sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in ETUs. The parity error is besides signaled during the guard time.

9.6.5.10. Smart Card Reader Line Control Register(Default Value: 0x0000_0000)

Offset: 0x0030			**Register Name: SCR_PAD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DSCVPPPP Direct Smart Card Vpp Pause/Prog. It provides direct access to SCVPPPP output.
6	R/W	0x0	DSCVPPEN Direct Smart Card Vpp Enable. It provides direct access to SCVPPEN output.
5	R/W	0x0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSVPPEN and DSVPPPP signals during activation and deactivation sequence.
4	R/W	0x0	DSCVCC Direct Smart Card VCC. When DIRACCPADS='1', the DSCVCC bit provides direct access to SCVCC pad.
3	R/W	0x0	DSCRST Direct Smart Card Clock. When DIRACCPADS='1', the DSCRST bit provides direct access to SCRST pad.
2	R/W	0x0	DSCCLK Direct Smart Card Clock. When DIRACCPADS='1', the DSCCLK bit provides direct access to SCCLK pad.
1	R/W	0x0	DSCIO Direct Smart Card Input/Output. When DIRACCPADS='1', the DSCIO bit provides direct access to SCIO pad.
0	R/W	0x0	DIRACCPADS

			Direct Access to Smart Card Pads. When high, it disables a serial interface functionality and enables direct control of the Smart Card pads using following 4 bits.

Note: This register provides direct access to Smart Card pads without serial interface assistance. You can use this register feature with synchronous and any other non-ISO 7816 and non-EMV cards.

9.6.5.11. Smart Card Reader FIFO Data Register(Default Value: 0x0000_0000)

Offset: 0x0100			**Register Name: SCR_FIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	FIFO_DATA This 8-bit register provides access to the RX and TX FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer.

9.7. EMAC

9.7.1. Overview

The Ethernet MAC(EMAC) controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M/1000M external PHY with MII/ RGMII interface in both full and half duplex mode. The Ethernet MAC-DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4K Byte TXFIFO and 16K Byte RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

Features:

- Supports 10/100/1000Mbps data transfer rates
- Supports MII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list (chained) descriptor chaining
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

9.7.2. Block Diagram

The EMAC Controller block diagram is shown below:

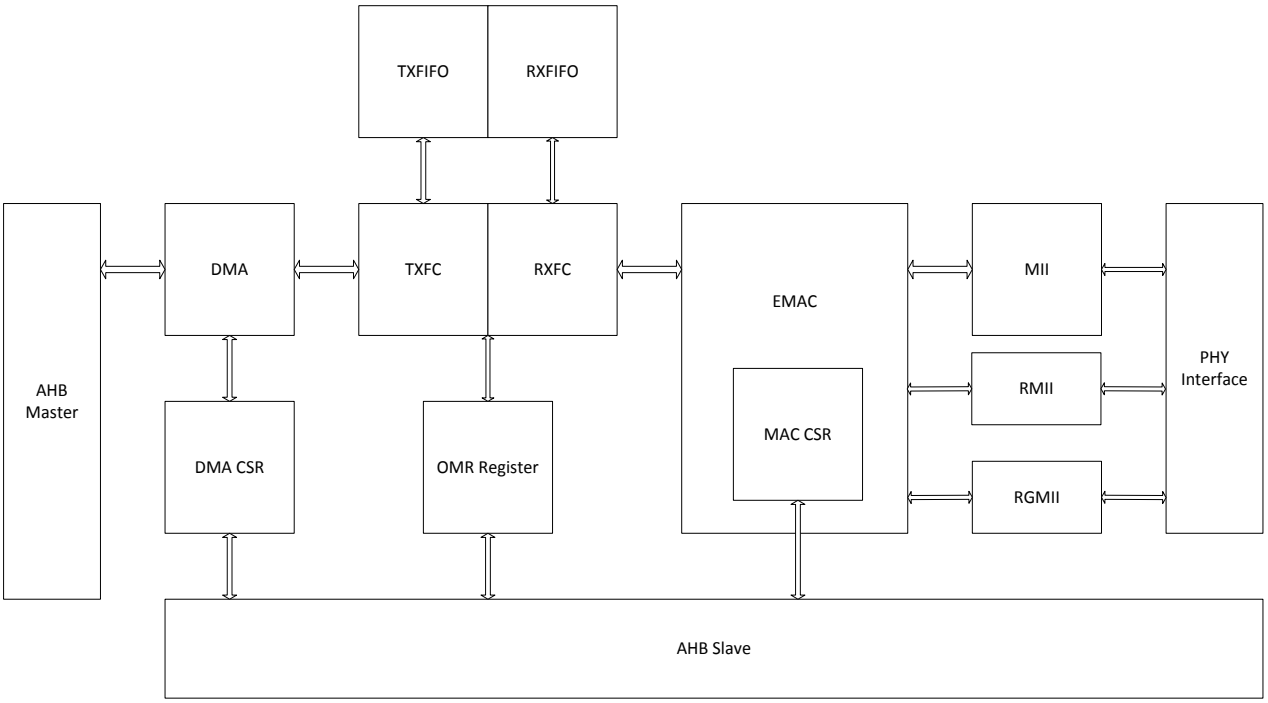


Figure 9-11. EMAC Block Diagram

9.7.3. Operations and Functional Descriptions

9.7.3.1. External Signals

The following table describes the pin list of EMAC.

Table 9-10. EMAC External Signals

Pin Name	Description	Type
RGMII_RXD3/MII_RXD3 /RMII_NULL	RGMII/MII Receive Data	I
RGMII_RXD2/MII_RXD2/ RMII_NULL	RGMII/MII Receive Data	I
RGMII_RXD1/MII_RXD1/ RMII_RXD1	RGMII/MII/RMII Receive Data	I
RGMII_RXD0/MII_RXD0/ RMII_RXD0	RGMII/MII/RMII Receive Data	I
RGMII_RXCK/MII_RXCK/ RMII_NULL	RGMII/MII Receive Clock	I
RGMII_RXCTL/MII_RXDV/ RMII_CRS_DV	RGMII Receive Control/MII Receive Enable/RMII Carrier Sense-Receive Data Valid	I
RGMII_NULL/MII_RXERR/ RMII_RXER	MII/RMII Receive Error	I

RGMII_TXD3/MII_TXD3/ RMII_NULL	RGMII/MII Transmit Data	O
RGMII_TXD2/MII_TXD2/ RMII_NULL	RGMII/MII Transmit Data	O
RGMII_TXD1/MII_TXD1/ RMII_TXD1	RGMII/MII/RMII Transmit Data	O
RGMII_TXD0/MII_TXD0/ RMII_TXD0	RGMII/MII/RMII Transmit Data	O
RGMII_NULL/MII_CRS/ RMII_NULL	MII Carrier Sense	I
RGMII_TXCK/MII_TXCK/ RMII_TXCK	RGMII/MII/RMII Transmit Clock: Output Pin for RGMII, Input Pin for MII/RMII	I/O
RGMII_TXCTL/MII_TXEN/ RMII_TXEN	RGMII Transmit Control/MII Transmit Enable/RMII Transmit Enable: Output Pin for RGMII/RMII, Input Pin for MII	I/O
RGMII_NULL/MII_TXERR/ RMII_NULL	MII Transmit Error	O
RGMII_CLKIN/MII_COL/ RMII_NULL	RGMII Transmit Clock from External/MII Collision Detect	I
MDC	RGMII/MII/RMII Management Data Clock	O
MDIO	RGMII/MII/RMII Management Data Input and Output	I/O

9.7.3.2. EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in figure 9-12. The address of each descriptor must be 32-bit aligned.

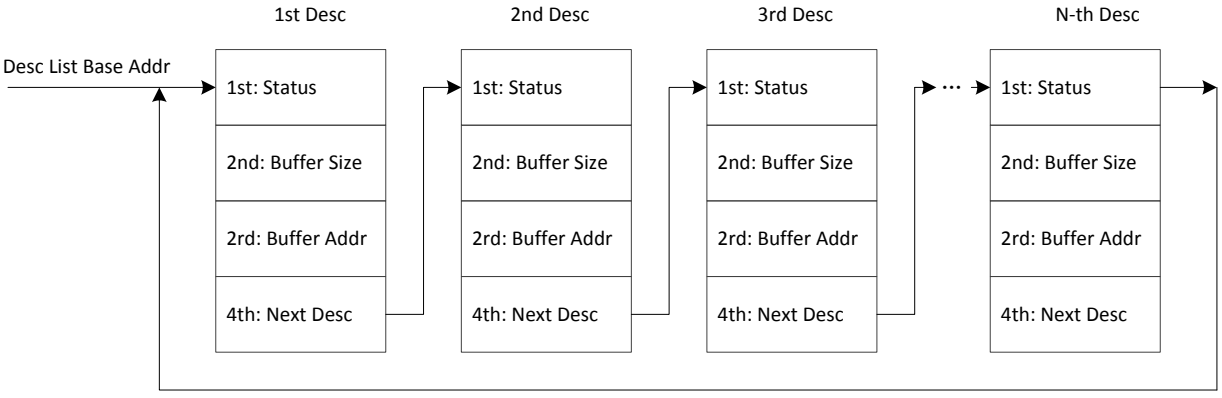


Figure 9-12. EMAC RX/TX Descriptor List

9.7.3.3. Transmit Descriptor

(1).1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved.
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

(2).2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved

10:0	BUF_SIZE The size of buffer specified by current descriptor.

(3).3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

(4).4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

9.7.3.4. Receive Descriptor

(1).1st Word of Receive Descriptor

Bits	Description
31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame don't pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame don't pass SA filter.
12	Reserved.
11	RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.

7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR When set, there is a late collision during reception in half-duplex mode.
5	Reserved.
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.
2	Reserved.
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

(2).2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When set and a frame have been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

(3).3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

(4).4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

9.7.4. Register List

Module Name	Base Address
EMAC	0x01C30000

Register Name	Offset	Description
BASIC_CTL_0	0x0000	Basic Control 0 Register
BASIC_CTL_1	0x0004	Basic Control 1 Register
INT_STA	0x0008	Interrupt Status Register
INT_EN	0x000C	Interrupt Enable Register
TX_CTL_0	0x0010	Transmit Control 0 Register
TX_CTL_1	0x0014	Transmit Control 1 Register
TX_FLOW_CTL	0x001C	Transmit Flow Control Register
TX_DMA_DESC_LIST	0x0020	Transmit Descriptor List Address Register
RX_CTL_0	0x0024	Receive Control 0 Register
RX_CTL_1	0x0028	Receive Control 1 Register
RX_DMA_DESC_LIST	0x0034	Receive Descriptor List Address Register
RX_FRM_FLT	0x0038	Receive Frame Filter Register
RX_HASH_0	0x0040	Hash Table 0 Register
RX_HASH_1	0x0044	Hash Table 1 Register
MII_CMD	0x0048	Management Interface Command Register
MII_DATA	0x004C	Management Interface Data Register
ADDR_HIGH_0	0x0050	MAC Address High Register 0
ADDR_LOW_0	0x0054	MAC Address High Register 0
ADDR_HIGH_x	0x0050+n*0x08	MAC Address High Register n(n=1~7)
ADDR_LOW_x	0x0054+n*0x08	MAC Address Low Register n(n=1~7)
TX_DMA_STA	0x00B0	Transmit DMA Status Register
TX_CUR_DESC	0x00B4	Current Transmit Descriptor Register
TX_CUR_BUF	0x00B8	Current Transmit Buffer Address Register
RX_DMA_STA	0x00C0	Receive DMA Status Register
RX_CUR_DESC	0x00C4	Current Receive Descriptor Register
RX_CUR_BUF	0x00C8	Current Receive Buffer Address Register
RGMII_STA	0x00D0	RGMII Status Register

9.7.5. Register Description

9.7.5.1. Basic Control 0 Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: BASIC_CTL_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000Mbps 11: 100Mbps 10: 10Mbps 01: Reserved

1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

9.7.5.2. Basic Control 1 Register(Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: BASIC_CTL_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI 0: RX DMA and TX DMA have same priority 1: RX DMA has priority over TX DMA
0	R/W	0x0	SOFT_RST When this bit is set, soft reset all registers and logic. All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.

9.7.5.3. Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	RGMII_LINK_STA_INT When this bit is asserted, the link status of RGMII interface is changed.
15:14	/	/	/
13	R	0x0	RX_EARLY_INT When this bit asserted, the RX DMA had filled the first data buffer of the receive frame.
12	R	0x0	RX_OVERFLOW_INT When this bit is asserted, the RX FIFO had an overflow error.
11	R	0x0	RX_TIMEOUT_INT When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R	0x0	RX_DMA_STOPPED_INT

			When this bit asserted, the RX DMA FSM is stopped.
9	R	0x0	RX_BUF_UA_INT When this asserted, the RX DMA can't acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when write to DMA_RX_START bit or next receive frame is coming.
8	R	0x0	RX_INT When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R	0x0	TX_EARLY_INT When this bit asserted , the frame is transmitted to FIFO totally.
4	R	0x0	TX_UNDERFLOW_INT When this bit is asserted, the TX FIFO had an underflow error.
3	R	0x0	TX_TIMEOUT_INT When this bit is asserted, the transmitter had been excessively active.
2	R	0x0	TX_BUF_UA_INT When this asserted, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when write to DMA_TX_START bit.
1	R	0x0	TX_DMA_STOPPED_INT When this bit is asserted, the TX DMA FSM is stopped.
0	R	0x0	TX_INT When this bit is asserted, a frame transmission is completed.

9.7.5.4. Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: INT_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN 0: Disable early receive interrupt enable 1: Enable early receive interrupt enable
12	R/W	0x0	RX_OVERFLOW_INT_EN 0: Disable overflow interrupt 1: Enable overflow interrupt
11	R/W	0x0	RX_TIMEOUT_INT_EN 0: Disable receive timeout interrupt 1: Enable receive timeout interrupt
10	R/W	0x0	RX_DMA_STOPPED_INT_EN

			0: Disable receive DMA FSM stopped interrupt 1: Enable receive DMA FSM stopped interrupt
9	R/W	0x0	RX_BUF_UA_INT_EN 0: Disable receive buffer unavailable interrupt 1: Enable receive buffer unavailable interrupt
8	R/W	0x0	RX_INT_EN 0: Disable receive interrupt 1: Enable receive interrupt
7:6			
5	R/W	0x0	TX_EARLY_INT_EN 0: Disable early transmit interrupt 1: Enable early transmit interrupt
4	R/W	0x0	TX_UNDERFLOW_INT_EN 0: Disable underflow interrupt 1: Enable underflow interrupt
3	R/W	0x0	TX_TIMEOUT_INT_EN 0: Disable transmit timeout interrupt 1: Enable transmit timeout interrupt
2	R/W	0x0	TX_BUF_UA_INT_EN 0: Disable transmit buffer available interrupt 1: Enable transmit buffer available interrupt
1	R/W	0x0	TX_DMA_STOPPED_INT_EN 0: Disable transmit DMA FSM stopped interrupt 1: Enable transmit DMA FSM stopped interrupt
0	R/W	0x0	TX_INT_EN 0: Disable transmit interrupt 1: Enable transmit interrupt

9.7.5.5. Transmit Control 0 Register(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: TX_CTL_0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable transmitter.

			0: Disable transmitter after current transmission 1: Enable
30	R/W	0x0	TX_FRM_LEN_CTL 0: Allow to transmit frames no more than 2,048 bytes (10,240 if JUMBO_FRM_EN is set) and cut off any bytes after that 1: Allow to transmit frames of up to 16,384 bytes
29:0	/	/	/

9.7.5.6. Transmit Control 1 Register(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: TX_CTL_1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START When set this bit, the TX DMA FSM will go no to work. It is cleared internally and always read a 0.
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission. 1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH The threshold value of TX DMA FIFO. When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD 0: Transmission starts after the number of data in TX DAM FIFO is greater than TX_TH 1: Transmission starts after a full frame located in TX DMA FIFO
0	R/W	0x0	FLUSH_TX_FIFO The functionality that flush the data in the TX FIFO. 0: Enable 1: Disable

9.7.5.7. Transmit Flow Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode. 0: Disable 1: Enable

9.7.5.8. Transmit DMA Descriptor List Address Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

9.7.5.9. Receive Control 0 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: RX_CTL_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable receiver

			0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL 0: Allow to receive frames less than or equal to 2,048 bytes (10,240 if JUMBO_FRM_EN is set) and cuts off any bytes received after that 1: Allow to receive frames of up to 16,384 bytes
29	R/W	0x0	JUMBO_FRM_EN When set, allows Jumbo frames of 9,018 bytes without reporting a giant frame error in the receive frame status.
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC When set, calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

9.7.5.10. Receive Control 1 Register(Default Value: 0x0000_0000)

Offset: 0x0028			**Register Name: RX_CTL_1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_DMA_START When set, the RX DMA will not go to work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL 0: Disable RX flow control 1: Enable RX flow control based on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT

23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT The threshold for deactivating flow control in both half-duplex mode and full-duplex mode. 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT The threshold for activating flow control in both half-duplex mode and full-duplex mode. 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB
19:6	/	/	/
5:4	R/W	0x0	RX_TH The threshold value of RX DMA FIFO. When RX_MD is 0, RX DMA starts to transfer data when the size of received frame in RX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 00: 64 01: 32 10: 96 11: 128
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes.
1	R/W	0x0	RX_MD 0: RX DMA reads data from RX DMA FIFO to host memory after the number of data in RX DAM FIFO is greater than RX_TH 1: RX DMA reads data from RX DMA FIFO to host memory after a complete frame has been written to RX DMA FIFO
0	R/W	0x0	FLUSH_RX_FRM The functionality that flush the frames when receive descriptors/buffers is unavailable. 0: Enable

			1: Disable

9.7.5.11. Receive DMA Descriptor List Address Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

9.7.5.12. Receive Frame Filter Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER 0: Enable address filter 1: Disable address filter
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST 0: Receive all broadcast frames 1: Drop all broadcast frames
16	R/W	0x0	RX_ALL_MULTICAST 0: Filter multicast frame according to HASH_MULTICAST 1: Receive all multicast frames
15:14	/	/	
13:12	R/W	0x0	CTL_FRM_FILTER 00, 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST 0: Filter multicast frames by comparing the DA field with the values in DA MAC address registers 1: Filter multicast frames according to the hash table
8	R/W	0x0	HASH_UNICAST 0: Filter unicast frames by comparing the DA field with the values in DA MAC address registers 1: Filter unicast frames according to the hash table

7	/	/	/
6	R/W	0x0	SA_FILTER_EN 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER 0: When the SA field of current frame matches the values in SA MAC address registers, it passes the SA filter 1: When the SA filed of current frame does not match the values in SA MAC address registers,, it passes the SA filter
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it pass the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

9.7.5.13. Receive Hash Table 0 Register(Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: RX_HASH_0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB_0 The upper 32 bits of hash table for receive frame filter.

9.7.5.14. Receive Hash Table 1 Register(Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: RX_HASH_1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB_1 The lower 32 bits of hash table for receive frame filter.

9.7.5.15. MII Command Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC clock divide ration(m). The source of MDC clock is AHB clock. 000: 16 001: 32 010: 64 011: 128 Others: Reserved
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR Select a PHY device from 32 possible candidates.
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR Select register in the selected PHY device
3:2	/	/	/
1	R/W	0x0	MII_WR 0: Read register in selected PHY and return data in EMAC_GMII_DATA 1: Write register in selected PHY using data in EMAC_GMII_DATA
0	R/W	0x0	MII_BUSY This bit indicates that a read or write operation is in progress. When prepared the data and register address for a write operation or the register address for a read operation, set this bit and start to access register in PHY. When this bit is cleared automatically, the read or write operation is over and the data in EMAC_GMII_DATA is valid for a read operation.

9.7.5.16. MII Data Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA The 16-bit data to be written to or read from the register in the selected PHY.

9.7.5.17. MAC Address 0 High Register(Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: ADDR0_HIGH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_0_HIGH The upper 16bits of the 1st MAC address.

9.7.5.18. MAC Address 0 Low Register(Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: ADDR0_LOW
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_0_LOW The lower 32bits of 1st MAC address.

9.7.5.19. MAC Address N High Register(Default Value: 0x0000FFFF)

Offset: 0x0050+N*0x08 (N=1~7)			Register Name: ADDRN_HIGH
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL 0: MAC address N(N: 1~7) is not valid, and it will be ignored by the address filter 1: MAC address N(N:1~7) is valid
30	R/W	0x0	MAC_ADDR_TYPE 1: MAC address N(N:1~7) is used to compare with the source address of the received frame 0: MAC address n(N:1~7) is used to compare with the destination address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC address byte control mask. The lower bit of mask controls the lower byte of in MAC address N(N:1~7). When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_N_HIGH The upper 16bits of the MAC address N(N:1~7).

9.7.5.20. MAC Address N Low Register(Default Value: 0xFFFF_FFFF)

Offset: 0x0054+N* 0x08 (N=1~7)			Register Name: ADDRN_LOW
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0xFFFFFFFF	MAC_ADDR_N_LOW The lower 32bits of MAC address N(N:1~7).

9.7.5.21. Transmit DMA Status Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The state of Transmit DMA FSM. 000: STOP: When reset or disable TX DMA 001: RUN_FETCH_DESC: Fetching TX DMA descriptor 010: RUN_WAIT_STA: Waiting for the status of TX frame 011: RUN_TRANS_DATA: Passing frame from host memory to TX DMA FIFO 111: RUN_CLOSE_DESC: Closing TX descriptor. 110: SUSPEND: TX descriptor unavailable or TX DMA FIFO underflow 100, 101: Reserved

9.7.5.22. Transmit DMA Current Descriptor Register(Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

9.7.5.23. Transmit DMA Current Buffer Address Register(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: TX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit DMA buffer

9.7.5.24. Receive DMA Status Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: RX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The state of RX DMA FSM. 000: STOP. When reset or disable RX DMA 001: RUN_FETCH_DESC. Fetching RX DMA descriptor

			011: RUN_WAIT_FRM. Waiting for frame 100: SUSPEND. RX descriptor unavailable 101: RUN_CLOSE_DESC. Closing RX descriptor 111: RUN_TRANS_DATA. Passing frame from host memory to RX DMA FIFO 010, 110: Reserved

9.7.5.25. Receive DMA Current Descriptor Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: RX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive descriptor

9.7.5.26. Receive DMA Current Buffer Address Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: RX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive DMA buffer

9.7.5.27. RGMII Status Register(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: RGMII_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface 0: Down 1: Up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz
0	R	0x0	RGMII_LINK_MD The link Mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

9.8. TSC

9.8.1. Overview

The transport stream controller(TSC) is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1.

The transport stream controller receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before the Packet to be store to memory by DMA, it can be pre-processing by the Transport Stream Descrambler.

The transport stream controller can be used for almost all multi-media application cases, example: DVB Set top Box, IPTV, Streaming-media Box, multi-media players and so on.

Features:

- Supports industry-standard AMBA Host Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus.
- Supports AHB 32-bit bus width
- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter for TSF
- Multiple transport stream packet (188, 192, 204) format support
- SPI and SSI timing parameters are configurable
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- Configurable SPI transport stream generator for streams in DRAM memory
- DMA is supported for transferring data
- Interrupt is supported
- Supports DVB-CSA V1.1 Descrambler

9.8.2. Block Diagram

Figure 9-13 shows a block diagram of the TSC.

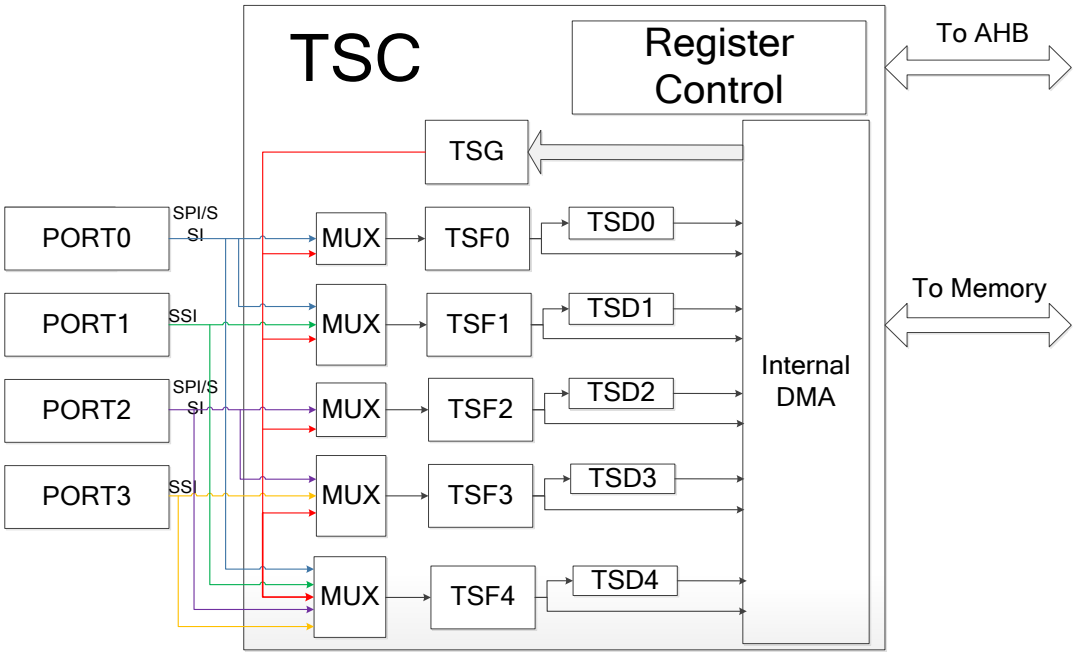


Figure 9-13. TSC Block Diagram

Note:

TSC – TS Controller

TSF – TS Filter

TSD – TS Descrambler

TSG – TS Generator

9.8.3. Operations and Functional Descriptions

9.8.3.1. External Signals

Table 9-11 describes the external signals of TSC.

Table 9-11. TSC External Signals

Pin Name	Description	Type
TS0_CLK	Transport Stream0 Clock	I
TS0_ERR	Transport Stream0 Error Indicate	I
TS0_SYNC	Transport Stream0 Sync	I
TS0_DVLD	Transport Stream0 Valid Signal	I
TS0_D[7:0]	Transport Stream0 Data	I
TS1_CLK	Transport Stream1 Clock	I
TS1_ERR	Transport Stream1 Error Indicate	I
TS1_SYNC	Transport Stream1 Sync	I
TS1_DVLD	Transport Stream1 Valid Signal	I
TS1_D0	Transport Stream1 Data	I

TS2_CLK	Transport Stream2 Clock	I
TS2_ERR	Transport Stream2 Error Indicate	I
TS2_SYNC	Transport Stream2 Sync	I
TS2_DVLD	Transport Stream2 Valid Signal	I
TS2_D[7:0]	Transport Stream2 Data	I
TS3_CLK	Transport Stream3 Clock	I
TS3_ERR	Transport Stream3 Error Indicate	I
TS3_SYNC	Transport Stream3 Sync	I
TS3_DVLD	Transport Stream3 Valid Signal	I
TS3_D0	Transport Stream3 Data	I

9.8.3.2. Clock Sources

The following table describes the clock sources of TSC.

Table 9-12. TSC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock,default value is 600MHz

9.8.3.3. TSC Timing Diagram

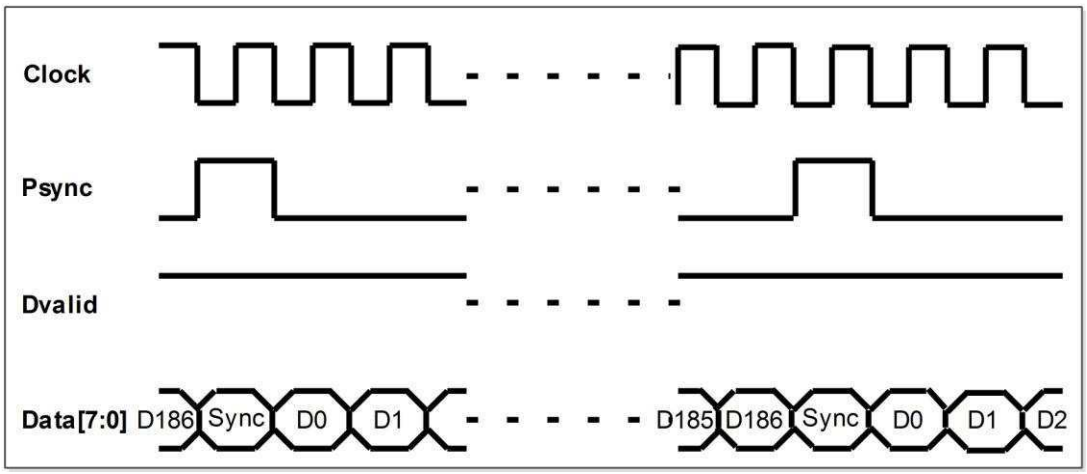


Figure 9-14. Input Timing for SPI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

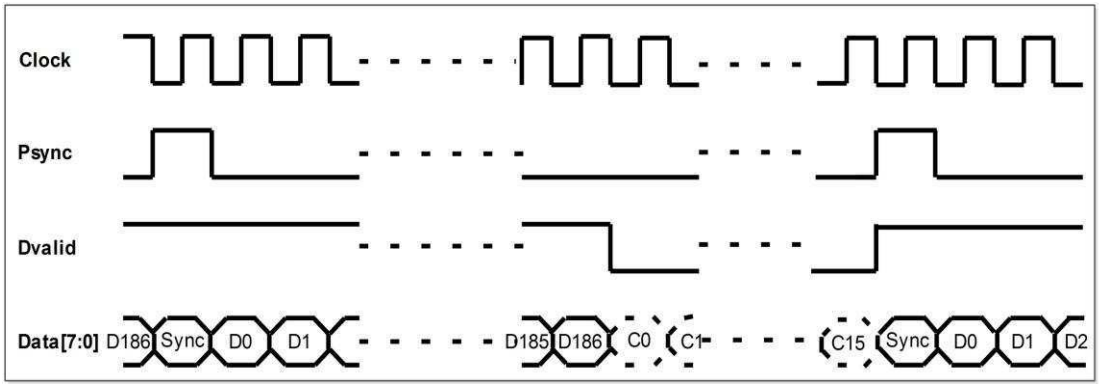


Figure 9-15. Alternative Input Timing for SPI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

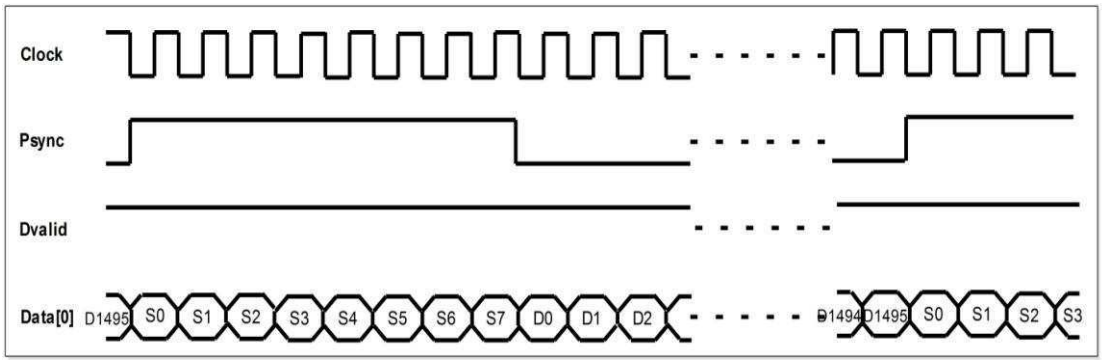


Figure 9-16. Alternative Input Timing for SSI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

9.8.4. Register List

Module Name	Base Address
TSC	0x01C06000
TSG	0x01C06040
TSF0	0x01C06100
TSD0	0x01C06180
TSF1	0x01C06200
TSD1	0x01C06280
TSF2	0x01C06300
TSD2	0x01C06380
TSF3	0x01C06400
TSD3	0x01C06480
TSF4	0x01C06500
TSD4	0x01C06580

Register Name	Offset	Description
TSC		
TSC_CTLR	TSC + 0x00	TSC Control Register
TSC_STAR	TSC + 0x04	TSC Status Register
TSC_PCTLR	TSC + 0x10	TSC Port Control Register
TSC_PPARR	TSC + 0x14	TSC Port Parameter Register
TSC_TSFMUXR	TSC + 0x20	TSC TSF Input Multiplex Control Register
TSC_OUTMUXR	TSC + 0x28	TSC Port Output Multiplex Control Register
TSC_INTSTSR	TSC + 0x30	TSC Interrupt Status Register
TSG		
TSG_CTLR	TSG + 0x00	TSG Control Register
TSG_PPR	TSG + 0x04	TSG Packet Parameter Register
TSG_STAR	TSG + 0x08	TSG Status Register
TSG_CCR	TSG + 0x0C	TSG Clock Control Register
TSG_BBAR	TSG + 0x10	TSG Buffer Base Address Register
TSG_BSZR	TSG + 0x14	TSG Buffer Size Register
TSG_BPR	TSG + 0x18	TSG Buffer Pointer Register
TSF		
TSF_CTLR	TSF + 0x00	TSF Control Register
TSF_PPR	TSF + 0x04	TSF Packet Parameter Register
TSF_STAR	TSF + 0x08	TSF Status Register
TSF_DIER	TSF + 0x10	TSF DMA Interrupt Enable Register
TSF_OIER	TSF + 0x14	TSF Overlap Interrupt Enable Register
TSF_DISR	TSF + 0x18	TSF DMA Interrupt Status Register
TSF_OISR	TSF + 0x1C	TSF Overlap Interrupt Status Register
TSF_PCRCR	TSF + 0x20	TSF PCR Control Register
TSF_PCRDR	TSF + 0x24	TSF PCR Data Register
TSF_CENR	TSF + 0x30	TSF Channel Enable Register
TSF_CPER	TSF + 0x34	TSF Channel PES Enable Register
TSF_CDER	TSF + 0x38	TSF Channel Descramble Enable Register
TSF_CINDR	TSF + 0x3C	TSF Channel Index Register
TSF_CCTLR	TSF + 0x40	TSF Channel Control Register
TSF_CSTAR	TSF + 0x44	TSF Channel Status Register
TSF_CCWIR	TSF + 0x48	TSF Channel CW Index Register
TSF_CPIDR	TSF + 0x4C	TSF Channel PID Register
TSF_CBBAR	TSF + 0x50	TSF Channel Buffer Base Address Register
TSF_CBSZR	TSF + 0x54	TSF Channel Buffer Size Register
TSF_CBWPR	TSF + 0x58	TSF Channel Buffer Write Pointer Register
TSF_CBRPR	TSF + 0x5C	TSF Channel Buffer Read Pointer Register
TSD		
TSD_CTLR	TSD + 0x00	TSD Control Register
TSD_STAR	TSD + 0x04	TSD Status Register
TSD_CWIR	TSD + 0x1C	TSD Control Word Index Register
TSD_CWR	TSD + 0x20	TSD Control Word Register

9.8.5. Register Description

9.8.5.1. TSC Control Register(Default Value: 0x0000_0000)

Offset: TSC+0x00			Register Name: TSC_CTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

9.8.5.2. TSC Status Register(Default Value: 0x0000_0000)

Offset: TSC+0x04			Register Name: TSC_STAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

9.8.5.3. TSC Port Control Register(Default Value: 0x0000_000A)

Offset: TSC+0x10			Register Name: TSC_PCTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x1	TSInPort3Ctrl TS Input Port3 Control 0: Reserved 1: SSI
2	R/W	0x0	TSInPort2Ctrl TS Input Port2 Control 0: SPI 1: SSI
1	R/W	0x1	TSInPort1Ctrl TS Input Port1 Control 0: Reserved 1: SSI
0	R/W	0x0	TSInPort0Ctrl TS Input Port0 Control 0: SPI 1: SSI

9.8.5.4. TSC Port Parameter Register(Default Value: 0x0000_0000)

<table>
<tr><td colspan="3">Offset: TSC+0x14</td><td>Register Name: TSC_PPARR</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:24</td><td>R/W</td><td>0x0</td><td>TSInPort3Par
TS Input Port3 Parameters

<table><tr><td>Bit</td><td>Definition</td></tr><tr><td>7:5</td><td>Reserved</td></tr><tr><td>4</td><td>SSI data order
0: MSB first for one byte data
1: LSB first for one byte data</td></tr><tr><td>3</td><td>CLOCK signal polarity
0: Rise edge capturing
1: Fall edge capturing</td></tr><tr><td>2</td><td>ERROR signal polarity
0: High level active
1: Low level active</td></tr><tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr><tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr></table></td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x0</td><td>TSInPort2Par
TS Input Port2 Parameters

<table><tr><td>Bit</td><td>Definition</td></tr><tr><td>7:5</td><td>Reserved</td></tr><tr><td>4</td><td>SSI data order
0: MSB first for one byte data
1: LSB first for one byte data</td></tr><tr><td>3</td><td>CLOCK signal polarity
0: Rise edge capturing
1: Fall edge capturing</td></tr><tr><td>2</td><td>ERROR signal polarity
0: High level active
1: Low level active</td></tr><tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr><tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr></table></td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>15:8</td><td>R/W</td><td>0x0</td><td>TSInPort1Par
TS Input Port1 Parameters
<table><tr><td>Bit</td><td>Definition</td></tr><tr><td>7:5</td><td>Reserved</td></tr><tr><td>4</td><td>SSI data order
0: MSB first for one byte data
1: LSB first for one byte data</td></tr><tr><td>3</td><td>CLOCK signal polarity
0: Rise edge capturing
1: Fall edge capturing</td></tr><tr><td>2</td><td>ERROR signal polarity
0: High level active
1: Low level active</td></tr><tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr><tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr></table></td></tr>
<tr><td>7:0</td><td>R/W</td><td>0x0</td><td>TSInPort0Par
TS Input Port0 Parameters
<table><tr><td>Bit</td><td>Definition</td></tr><tr><td>7:5</td><td>Reserved</td></tr><tr><td>4</td><td>SSI data order
0: MSB first for one byte data
1: LSB first for one byte data</td></tr><tr><td>3</td><td>CLOCK signal polarity
0: Rise edge capturing
1: Fall edge capturing</td></tr><tr><td>2</td><td>ERROR signal polarity
0: High level active
1: Low level active</td></tr><tr><td>1</td><td>DVALID signal polarity
0: High level active
1: Low level active</td></tr><tr><td>0</td><td>PSYNC signal polarity
0: High level active
1: Low level active</td></tr></table></td></tr>
</table>

9.8.5.5. TSC TSF Input Multiplex Control Register(Default Value: 0x0000_0000)

Offset: TSC+0x20			Register Name: TSC_TSFMUXR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	TSF4InputMuxCtrl TSF4 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port0 0010: Data from TS IN Port1 0011: Data from TS IN Port2 0100: Data from TS IN Port3 Others: Reserved
15:12	R/W	0x0	TSF3InputMuxCtrl TSF3 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port2 0010: Data from TS IN Port3 Others: Reserved
11:8	R/W	0x0	TSF2InputMuxCtrl TSF2 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port2 Others: Reserved
7:4	R/W	0x0	TSF1InputMuxCtrl TSF1 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port0 0010: Data from TS IN Port1 Others: Reserved
3:0	R/W	0x0	TSF0InputMuxCtrl TSF0 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port0 Others: Reserved

9.8.5.6. TSC Port Output Multiplex Control Register(Default Value: 0x0000_0000)

Offset: TSC+0x28	Register Name: TSC_TSFMUXR

Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

9.8.5.7. TSC Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSC+0x30			Register Name: TSC_INTSTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
16	R	0x0	TSG Interrupt Global Status When all TSG interrupt status bits are cleared,the bit will be cleared by hardware.
15:5	/	/	/
4	R	0x0	TSF4 Interrupt Global Status When all TSF4 interrupt status bits are cleared,the bit will be cleared by hardware.
3	R	0x0	TSF3 Interrupt Global Status When all TSF3 interrupt status bits are cleared,the bit will be cleared by hardware.
2	R	0x0	TSF2 Interrupt Global Status When all TSF2 interrupt status bits are cleared,the bit will be cleared by hardware.
1	R	0x0	TSF1 Interrupt Global Status When all TSF1 interrupt status bits are cleared,the bit will be cleared by hardware.
0	R	0x0	TSF0 Interrupt Global Status When all TSF0 interrupt status bits are cleared,the bit will be cleared by hardware.

9.8.5.8. TSG Control and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x00			Register Name: TSC_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	TSGSts Status for TS Generator 00: IDLE state 01: Running state 10: PAUSE state Others: Reserved
23:10	/	/	/
9	R/W	0x0	TSGLBufMode Loop Buffer Mode

			When set to '1', the TSG external buffer is in loop mode.
8	R/W	0x0	TSGSyncByteChkEn Sync Byte Check Enable Enable/Disable check SYNC byte for receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is receiver, TS Generator would come into PAUSE state. If the correspond interrupt is enable, the interrupt would happen.
7:3	/	/	/
2	R/W	0x0	TSGPauseBit Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finishing this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0x0	TSGStopBit Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finishing this operation, this bit will clear to zero by hardware.
0	R/W	0x0	TSGStartBit Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

9.8.5.9. TSG Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSG+0x04			**Register Name: TSG_PPR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0x0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position **Note:** This bit is only used for 192 bytes packet size.

6:2	/	/	/
1:0	R/W	0x0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes Others: Reserved

9.8.5.10. TSG Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x08			**Register Name: TSG_IESR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSGEndIE TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0x0	TSGFFIE TS Generator (TSG) Full Finish Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSGHFIE TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	TSGErrSyncByteIE TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0x0	TSGEndSts TS Generator (TSG) End Status Write ‘1’ to clear it.
2	R/W	0x0	TSGFFSts TS Generator (TSG) Full Finish Status Write ‘1’ to clear it.
1	R/W	0x0	TSGHFSts

			TS Generator (TSG) Half Finish Status Write '1' to clear it.
0	R/W	0x0	TSGErrSyncByteSts TS Generator (TSG) Error Sync Byte Status Write '1' to clear it.

9.8.5.11. TSG Clock Control Register(Default Value: 0x0000_0000)

Offset: TSG+0x0C			Register Name: TSG_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	TSGCDF_N TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSGCDF_D TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(8*(D+1)). Fi is the input special clock of TSC, and D must not less than N.

9.8.5.12. TSG Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSG+0x10			Register Name: TSG_BBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TSGBufBase Buffer Base Address This value is a start address of TSG buffer. **Note:** This value should be 4-word (16Bytes) align, and the lowest 4 bits of this value should be zero.

9.8.5.13. TSG Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSG+0x14			Register Name: TSG_BSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	TSGBufSize Data Buffer Size for TS Generator It is in byte unit. The size should be 4-word (16Bytes) align, and the lowest 4 bits should be zero.

9.8.5.14. TSG Buffer Point Register(Default Value: 0x0000_0000)

Offset: TSG+0x18			Register Name: TSG_BPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	TSGBufPtr Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

9.8.5.15. TSF Control and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x00			Register Name: TSF_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	TSF Enable 0: Disable TSF Input 1: Enable TSF Input
1	/	/	/
0	R/W	0x0	TSFGSR TSF Global Soft Reset Writing '1' by software will reset all status and state machine of TSF. And it is cleared by hardware after reset. Writing '0' by software has no effect.

9.8.5.16. TSF Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSF+0x04			Register Name: TSF_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LostSyncThd Lost Sync Packet Threshold It is used for packet sync lost by checking the value of sync byte.
27:24	R/W	0x0	SyncThd Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0x0	SyncMthd Packet Sync Method 00: By PSYNC signal

			01: By Sync byte 10: By both PSYNC and Sync Byte 11: Reserved
7	R/W	0x0	SyncBytePos Sync Byte Position 0: The 1st byte position 1: The 5th byte position **Note:** This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PktSize Packet Size Byte Size for one TS packet 00: 188 bytes 01: 192 bytes 10: 204 bytes 11: Reserved

9.8.5.17. TSF Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x08			**Register Name: TSF_IESR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSFFOIE TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	TSFPPDIE TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSFCOIE TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable 1: Enable
16	R/W	0x0	TSFCDIE TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable

			1: Enable
15:4	/	/	/
3	R/W	0x0	TSFFOIS TS PID Filter (TSF) Internal FIFO Overrun Status Write '1' to clear it.
2	R/W	0x0	TSFPPDIS TS PCR Packet Found Status When it is '1', one TS PCR Packet is found. Write '1' to clear it.
1	R	0x0	TSFCOIS TS PID Filter (TSF) Channel Overlap Status It is global status for 32 channel. It would clear to zero after all channels status bits are cleared.
0	R	0x0	TSFCDIS TS PID Filter (TSF) Channel DMA status It is global status for 32 channel. It would clear to zero after all channels status bits are cleared.

9.8.5.18. TSF DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x10			**Register Name: TSF_DIER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMAIE DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

9.8.5.19. TSF Overlap Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x14			**Register Name: TSF_OIER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	OLPIE Overlap Interrupt Enable Overlap interrupt enable bits for channel 0~31.

9.8.5.20. TSF DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x18			**Register Name: TSF_DISR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMAIS DMA Interrupt Status DMA interrupt status bits for channel 0~31. Set by hardware, and write 1 to clear it by software. When both these bits and the corresponding DMA Interrupt Enable bits set,

			the TSF interrupt will generate.

9.8.5.21. TSF Overlap Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x1C			Register Name: TSF_OISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	OLPIS Overlap Interrupt Status Overlap interrupt status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

9.8.5.22. TSF PCR Control Register(Default Value: 0x0000_0000)

Offset: TSF+0x20			Register Name: TSF_PCRCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PCRDE PCR Detecting Enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0x0	PCRCIND Channel Index m for detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0x0	PCRLSB PCR Contest LSB 1 bit PCR[0]

9.8.5.23. TSF PCR Data Register(Default Value: 0x0000_0000)

Offset: TSF+0x24			Register Name: TSF_PCRDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PCRMSB PCR Data High 32 bits PCR[33:1]

9.8.5.24. TSF Channel Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x30			Register Name: TSF_CENR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FilterEn Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, internal status of the corresponding filter channel will be reset.

9.8.5.25. TSF PES Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x34			Register Name: TSF_CPER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PESEn PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

9.8.5.26. TSF Channel Descramble Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x38			Register Name: TSF_CDER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DescEn Descramble Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

9.8.5.27. TSF Channel Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x3C			Register Name: TSF_CINDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/

4:0	R/W	0x0	CHIND Channel Index This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is 0x40~0x7f.

9.8.5.28. TSF Channel Control Register(Default Value: 0x0000_0000)

Offset: TSF+0x40			Register Name: TSF_CCTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

9.8.5.29. TSF Channel Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x44			Register Name: TSF_CSTAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

9.8.5.30. TSF Channel CW Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x48			Register Name: TSF_CCWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	CWIND Related Control Word Index Index to the control word used by this channel when Descramble Enable of this channel enable. This value is useless when the corresponding Descramble Enable is ‘0’.

9.8.5.31. TSF Channel PID Register(Default Value: 0x1FFF_0000)

Offset: TSF+0x4C			Register Name: TSF_CPIDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1FFF	PIDMSK Filter PID Mask for Channel
15:0	R/W	0x0	PIDVAL Filter PID value for Channel

9.8.5.32. TSF Channel Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSF+0x50			Register Name: TSF_CBBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:0	R/W	0x0	TSFBufBAddr Data Buffer Base Address for Channel It is 4-word (16Bytes) align address. The LSB four bits should be zero.

9.8.5.33. TSF Channel Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSF+0x54			Register Name: TSF_CBSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CHDMAIntThd DMA Interrupt Threshold for Channel The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 00: 1/2 data buffer packet size 01: 1/4 data buffer packet size 10: 1/8 data buffer packet size 11: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0x0	CHBufPktSz Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 bytes. The maximum buffer size is 2MB. This size should be 4-word (16Bytes) aligned. The LSB four bits should be zero.

9.8.5.34. TSF Channel Write Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x58			Register Name: TSF_CBWPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BufWrPtr Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by

			software during the corresponding channel is enabled.

9.8.5.35. TSF Channel Read Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x5C			Register Name: TSF_CBRPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BufRdPtr Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is read.

9.8.5.36. TSD Control Register(Default Value: 0x0000_0000)

Offset: TSD+0x00			Register Name: TSD_CTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	DescArith Descramble Arithmetic 00: DVB CSA V1.1 Others: Reserved

9.8.5.37. TSD Status Register(Default Value: 0x00000000)

Offset: TSD+0x04			Register Name: TSD_STAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

9.8.5.38. TSD Control Word Index Register(Default Value: 0x0000_0000)

Offset: TSD+0x1C			Register Name: TSD_CWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
6:4	R/W	0x0	CWI Control Word Index This value is the Control index for Control word access. Range is from 0x0 to 0x7.
3:2	/	/	/
1:0	R/W	0x0	CWII Control Word Internal Index

			00: Odd Control Word Low 32-bit, OCW[31:0] 01: Odd Control Word High 32-bit, OCW[63:32] 10: Even Control Word Low 32-bit, ECW[31:0] 11: Even Control Word High 32-bit, ECW[63:0]

9.8.5.39. TSD Control Word Register(Default Value: 0x0000_0000)

Offset: TSD+0x20			Register Name: TSD_CWR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CWD Content of Control Word corresponding to the **TSD_CWIR** value

Chapter 10 Electrical Characteristics

This section describes electrical characteristics of H5 processor.

10.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 10-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 10-1. Absolute Maximum Ratings

Symbol	Parameter		MIN	Max	Unit
$I_{I/O}$	In/Out Current for Input and Output		-40	40	mA
T_{STG}	Storage Temperature		-40	125	°C
AVCC	Power Supply for Analog Part		-0.3	3.4	V
EPHY-VCC	Power Supply for EPHY		-0.3	3.8	V
EPHY-VDD	Power Supply for EPHY		-0.3	1.4	V
HVCC	Power Supply for HDMI		-0.3	3.6	V
V33-TV	Power Supply for TV		-0.3	3.6	V
VCC-IO	Power Supply for Port A		-0.3	3.6	V
VCC-PC	Power Supply for Port C		-0.3	3.6	V
VCC-PD	Power Supply for Port D		-0.3	3.6	V
VCC-PG	Power Supply for Port G		-0.3	3.6	V
VCC-PLL	Power Supply for System PLL		-0.3	3.6	V
VCC-RTC	Power Supply for RTC		-0.3	3.6	V
VCC-USB	Power Supply for USB		-0.3	3.6	V
VCC-DRAM	Power Supply for DDR3/DDR3L		-0.3	1.65	V
VDD-CPUS	Power Supply for CPUS		-0.3	1.5	V
VDD-CPUX	Power Supply for CPU		-0.3	1.5	V
VDD-EFUSE	Power Supply for EFUSE		-0.3	3.6	V
VDD-SYS	Power Supply for System		-0.3	1.4	V
V_{ESD}	Electrostatic Discharge	Human Body Model(HBM)(1)	-4000	4000	V
		Charged Device Model(CDM)(2)	-250	250	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(3)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(4)		Pass		

(1). Test method: JEDEC JS-001-2012(Class-3A). JEDEC publication JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2). Test method: JESD22-C101F(Class-C1). JEDEC publication JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3). Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

(4). Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

10.2. Recommended Operating Conditions

All H5 modules are used under the operating Conditions contained in Table 10-2.

Table 10-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
Tj	Junction Temperature Range	TBD	-	TBD	°C
AVCC	Power Supply for Analog Part	-	3.3	-	V
EPHY-VCC	3.3V Power Supply for EPHY	3.0	3.3	3.6	V
EPHY-VDD	1.1V Power Supply for EPHY	1.0	1.1	1.2	V
HVCC	Power Supply for HDMI	3.24	3.3	3.36	V
V33-TV	Power Supply for TV	3.24	3.3	3.36	V
VCC-IO	Power Supply for 3.3V Digital Part	3.0	3.3	3.6	V
VCC-PC	Power Supply for Port C	1.7	1.8~3.3	3.6	V
VCC-PD	Power Supply for Port D	2.25	2.5~3.3	3.6	V
VCC-PG	Power Supply for Port G	1.7	1.8~3.3	3.6	V
VCC-PLL	Power Supply for System PLL	3.0	-	3.3	V
VCC-RTC	Power Supply for RTC	3.0	-	3.3	V
VCC-USB	Power Supply for USB	3.0	3.3	3.6	V
VCC-DRAM	Power Supply for DDR3 IO Domain	1.425	1.5	1.575	V
	Power Supply for DDR3L IO Domain	1.283	1.35	1.575	V
VDD-CPUS	Power Supply for CPUS	1.04	1.1	1.4	V
VDD-CPUX	Power Supply for CPU	1.1	1.1	1.4	V
VDD-EFUSE	Power Supply for EFUSE	-	3.3	-	V
VDD-SYS	Power Supply for System	1.1	1.2	1.3	V

10.3. DC Electrical Characteristics

Table 10-3 summarizes the DC electrical characteristics of H5.

Table 10-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ
R_{PD}	Input pull-down resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA

I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO - 0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

10.4. ADC Electrical Characteristics

KEYADC is an analog-to-digital(ADC) converter for key application. Table 10-4 lists KEYADC electrical characteristics.

Table 10-4. KEYADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	0.667*AVCC	V
Quantizing Error	-	1	-	LSB
Clock Frequency	-	-	250	Hz
Conversion Time	-	14	-	ADC Clock Cycles

10.5. Oscillator Electrical Characteristics

H5 contains two external input clocks:X24MIN and X32KIN, two output clocks:X24MOUT and X32KOUT.The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN.Table 10-5 lists the 24MHz crystal specifications.

Table 10-5. 24MHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25 °C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
P_{ON}	Drive Level	-	-	300	uW
C_L	Equivalent Load Capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	-	25	-	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	5	6.5	7.5	pF

R_{BIAS}	Internal Bias Resistor	0.5	0.6	0.7	MΩ

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. Table 10-6 lists the 32768Hz crystal specifications.

Table 10-6. 32768Hz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	32768	-	Hz
t_{ST}	Startup Time	-	-	–	ms
	Frequency Tolerance at 25 °C	-40	-	+40	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
P_{ON}	Drive Level	-	-	50	uW
C_L	Equivalent Load Capacitance	-	-	-	pF
R_S	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

10.6. Maximum Current Consumption

Table 10-7 lists the peak power consumption of H5.

Table 10-7. Maximum Current Consumption

Parameter	Sub Parameter	Power Supply	Condition	Min	Typ	Max	Unit
Internal Core Power	CPU	VDD-CPUX	@1.1V	-	-	TBD	mA
	SYS	VDD-SYS	@1.2V	-	-	TBD	mA
GPIO Power		VCC-IO, VCC-PC, VCC-PD, VCC-PG	@3.3V @2.5V @1.8V	-	-	TBD	mA
Memory I/O Power		VCC-DRAM	@1.5V	-	-	TBD	mA
Oscillator		VCC-PLL	@3.3V	-	-	TBD	mA
USB 3.0V Power of PHY		VCC-USB	@3.3V	-	-	TBD	mA
HDMI		HVCC	@3.3V	-	-	TBD	mA
RTC Power		VCC-RTC	@3.3V	-	-	TBD	mA
ADC Analog Power		AVCC	@3.3V	-	-	TBD	mA
DAC Analog Power		AVCC	@3.3V	-	-	TBD	mA
PLL Power		VCC-PLL	@3.3V	-	-	TBD	mA

10.7. External Memory AC Electrical Characteristics

10.7.1. Nand Flash AC Electrical Characteristics

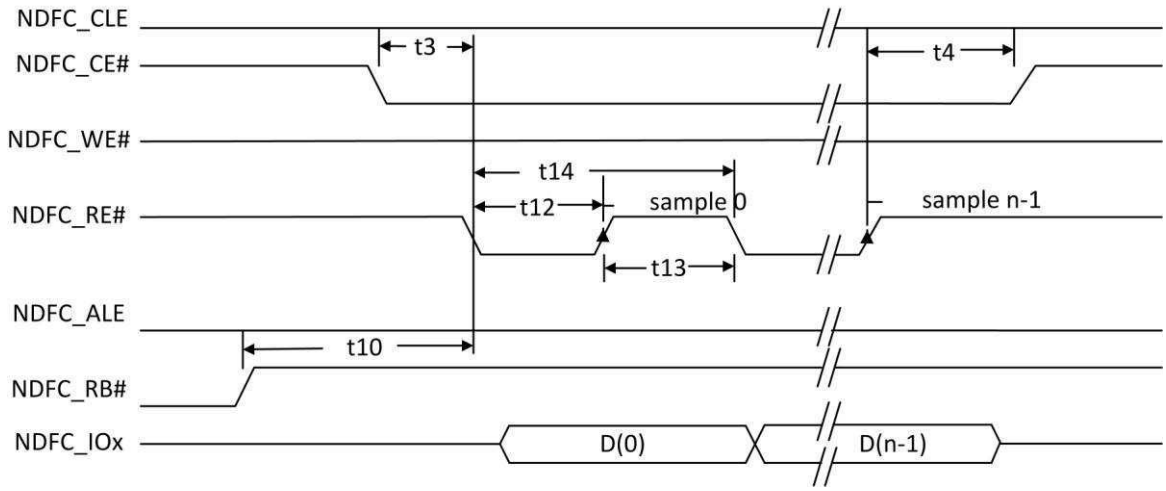


Figure 10-1. Conventional Serial Access Cycle Timing (SAM0)

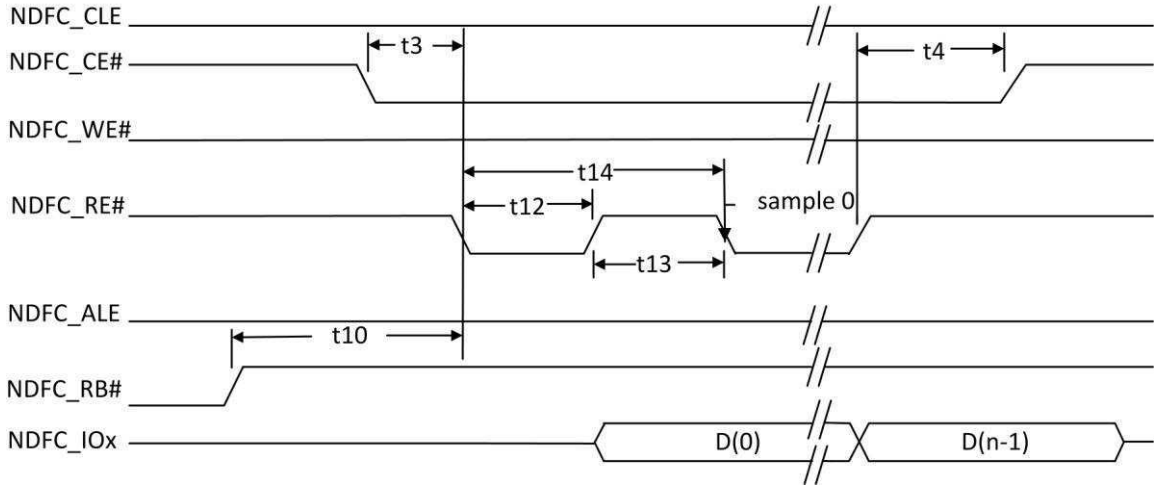


Figure 10-2. EDO Type Serial Access after Read Cycle Timing (SAM1)

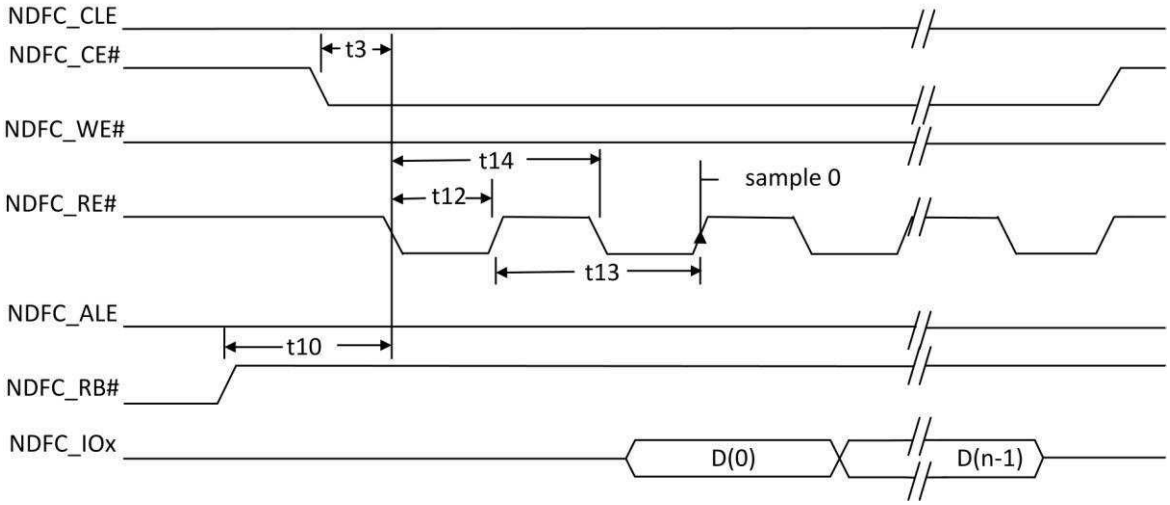


Figure 10-3. Extending EDO Type Serial Access Mode Timing (SAM2)

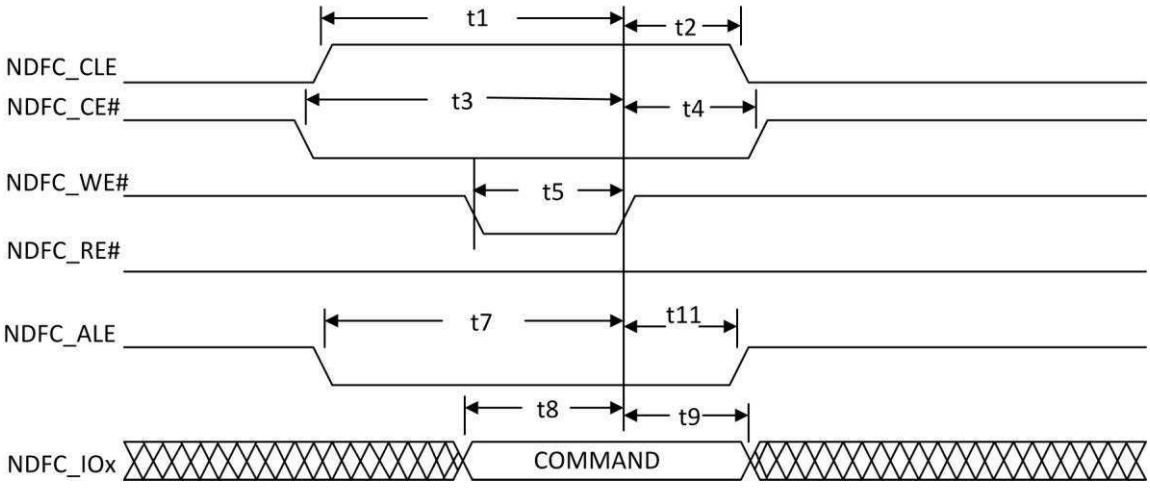


Figure 10-4. Command Latch Cycle Timing

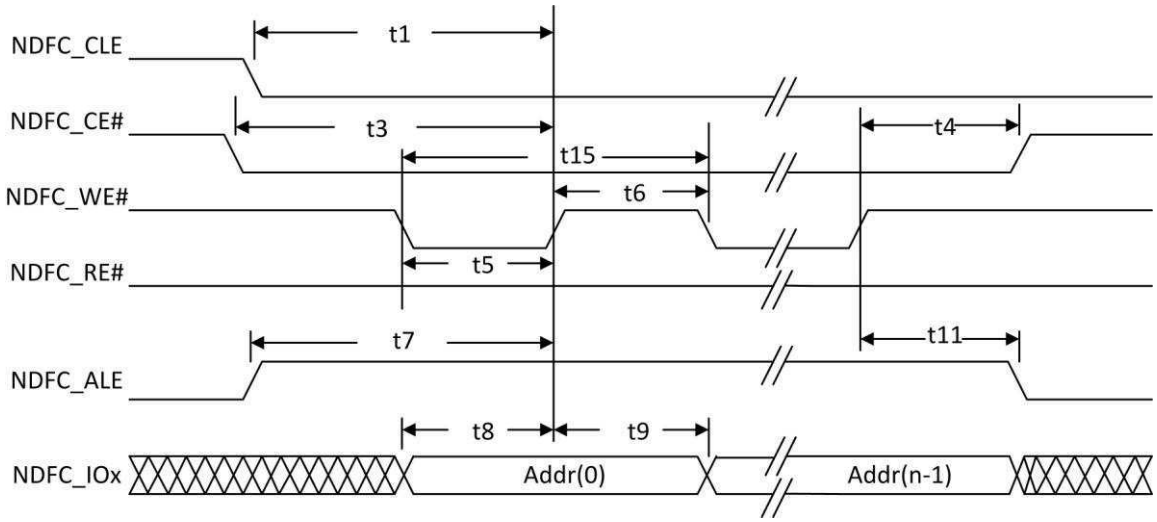


Figure 10-5. Address Latch Cycle Timing

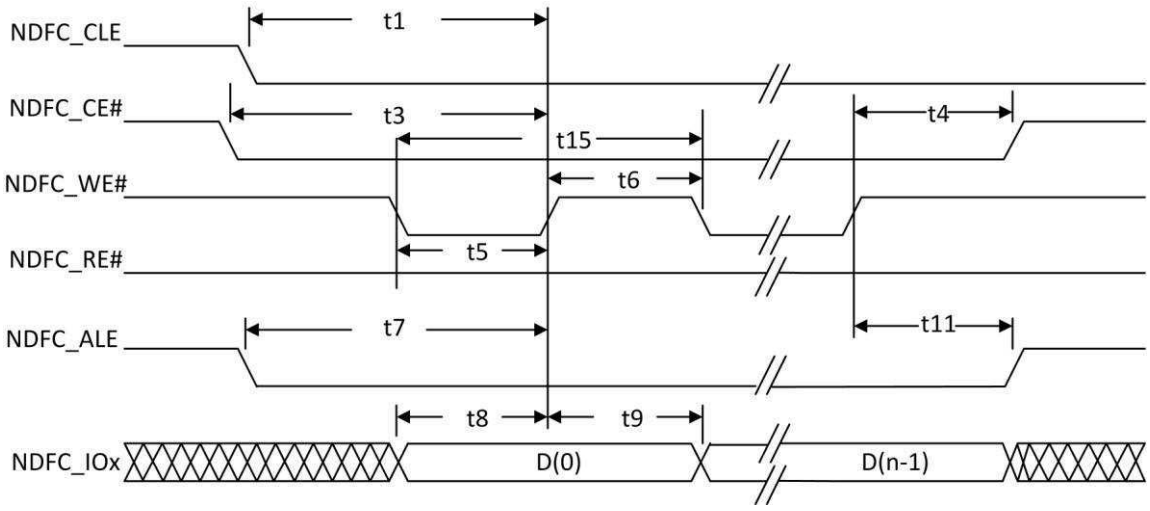


Figure 10-6. Write Data to Flash Cycle Timing

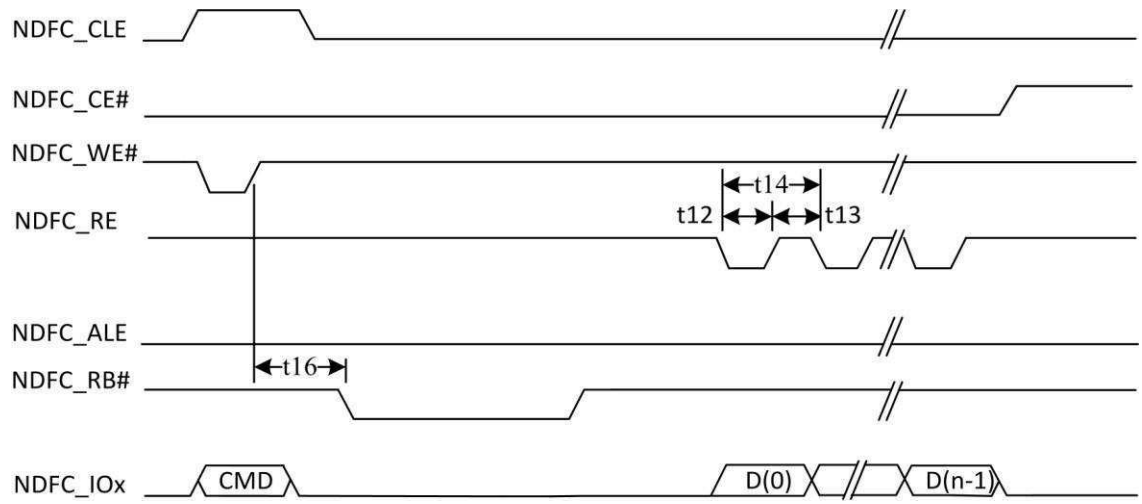


Figure 10-7. Waiting R/B# Ready Timing

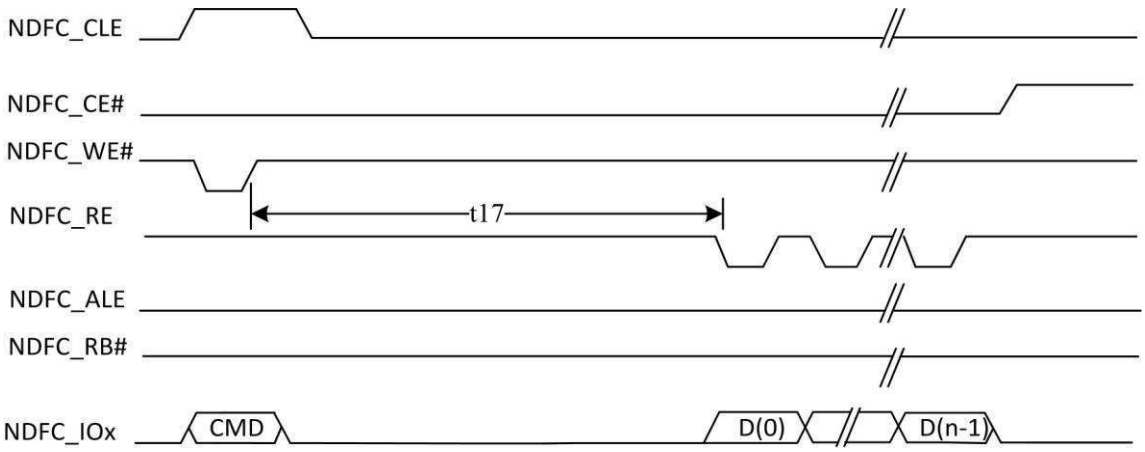


Figure 10-8. WE# High to RE# Low Timing

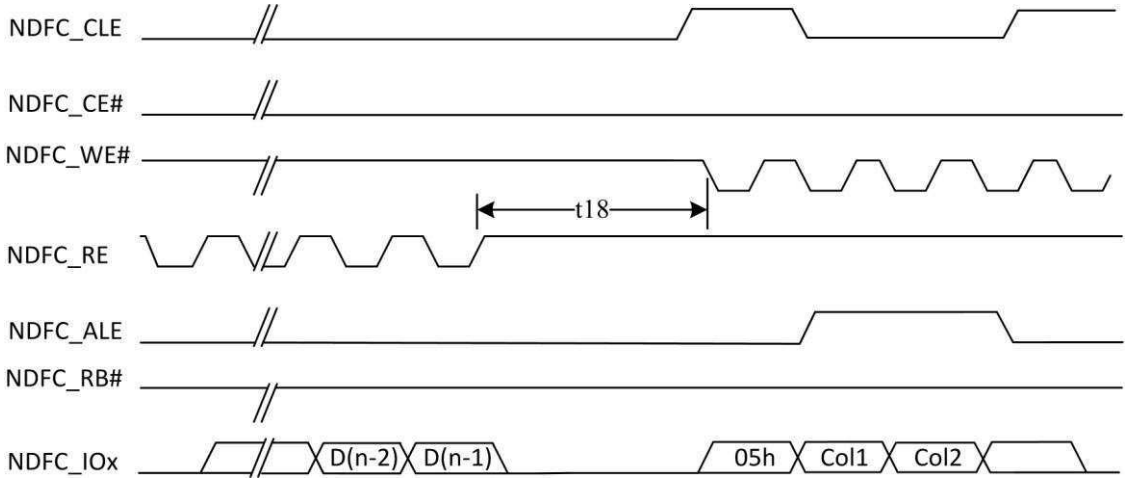


Figure 10-9. RE# High to WE# Low Timing

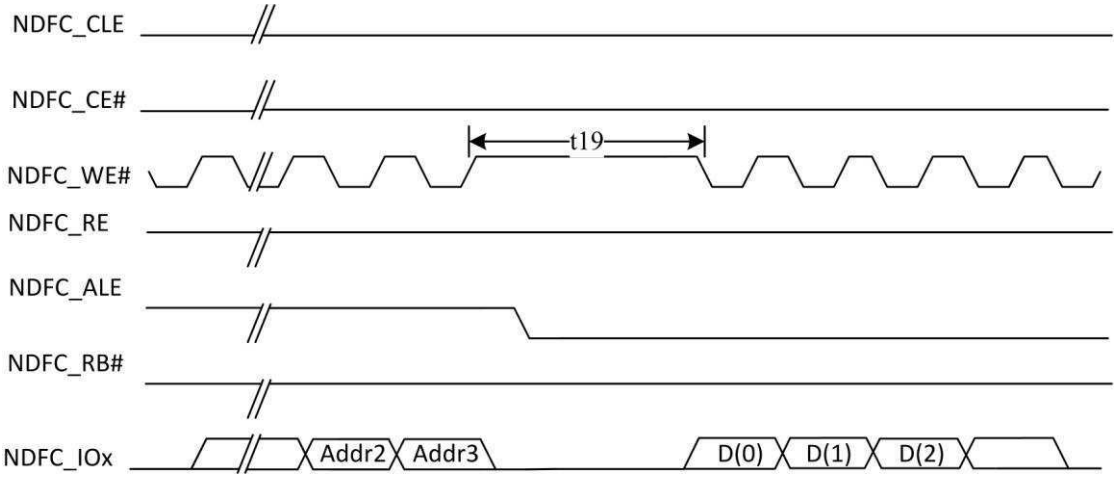


Figure 10-10. Address to Data Loading Timing

Table 10-8. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T(1)	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns

NOTE (1):T is the cycle of clock.

NOTE (2),(3),(4),(5): This values is configurable in Nand flash controller. The value of T_WB could be 28T/44T/60T/76T, the value of T_WHR could be 0T/12T/28T/44T, the value of T_RHW could be 8T/24T/40T/56T, the value of T_ADL could be 0T/12T/28T/44T.

10.7.2. SMHC AC Electrical Characteristics

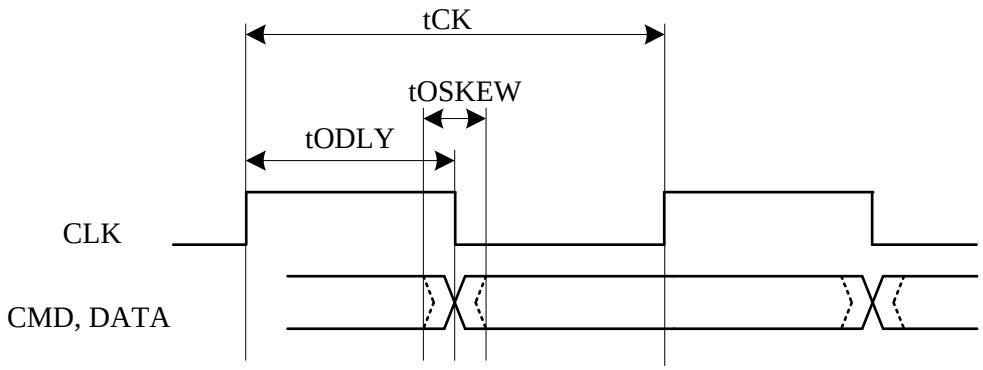


Figure 10-11. SMHC in SDR Mode Output Timing

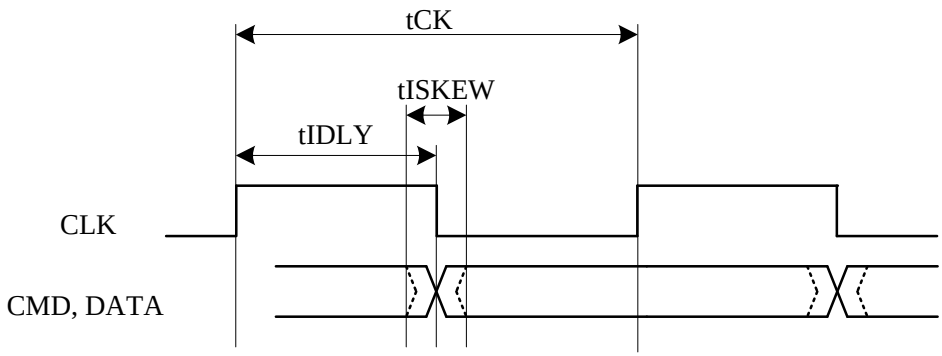


Figure 10-12. SMHC in SDR Mode Input Timing

Table 10-9. SMHC Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
CMD, Data output delay time	tODLY	-	-	12	ns
Data output delay skew time	tOSKEW	-	-	0.5	ns
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay.	tIDLY	-	-	21	ns
Data input skew time in SDR mode	tISKEW	-	-	0.8	ns
Note (1): Output CMD, DATA is referenced to CLK.					

10.8. External Peripheral AC Electrical Characteristics

10.8.1. LCD AC Electrical Characteristics

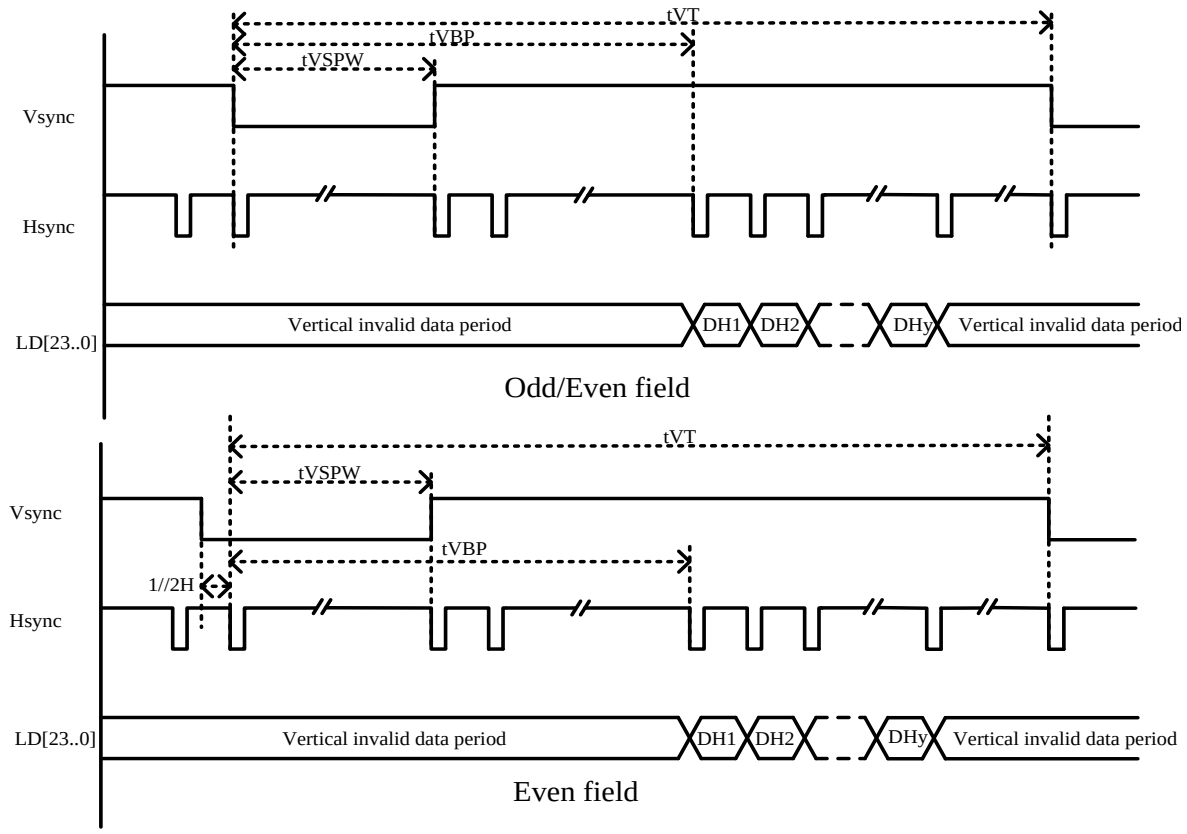


Figure 10-13. HV_IF Interface Vertical Timing

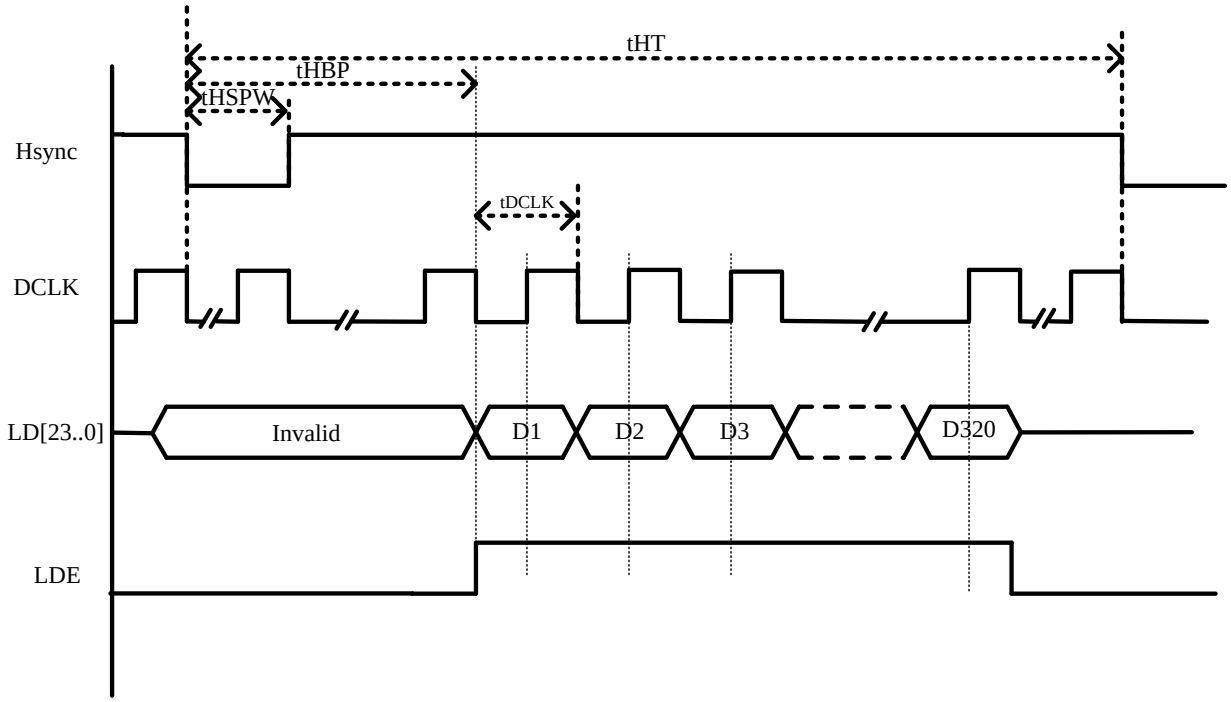


Figure 10-14. HV_IF Interface Parallel Mode Horizontal Timing

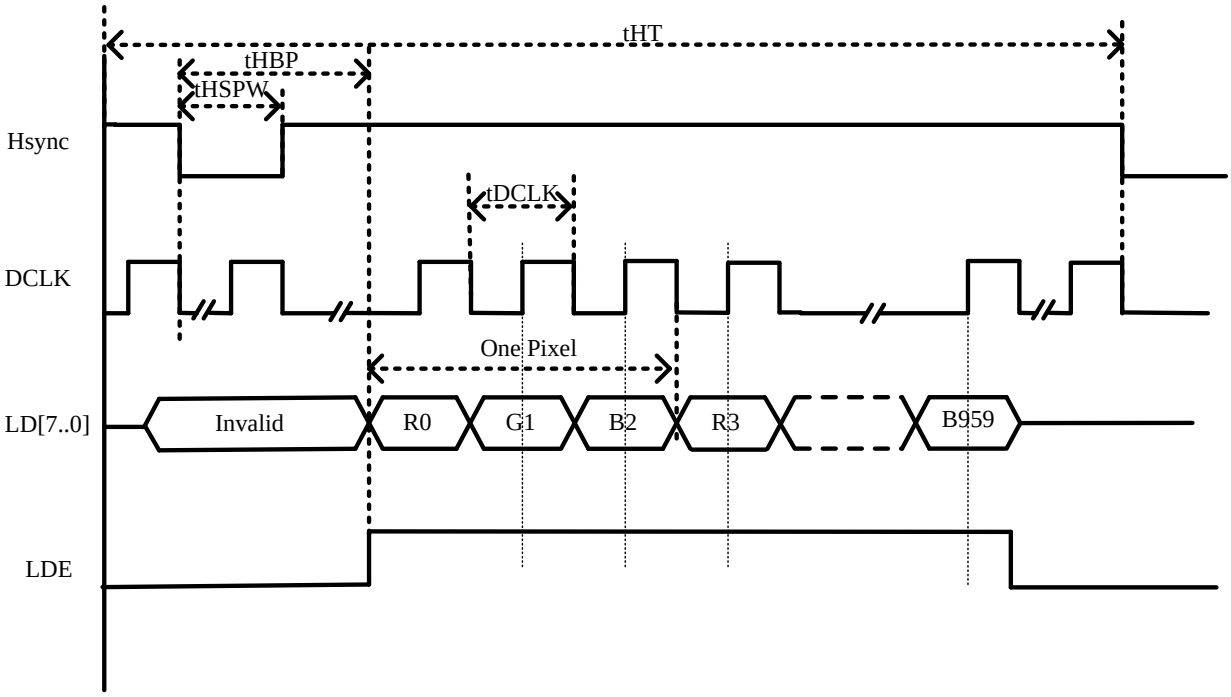


Figure 10-15. HV_IF Interface Serial Mode Horizontal Timing

Table 10-10. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK

HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

Note:

(1). Vsync: Vertical sync, indicates one new frame

(2). Hsync: Horizontal sync, indicate one new scan line

(3). DCLK: Dot clock, pixel data are sync by this clock

(4). LDE: LCD data enable

(5). LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel

10.8.2. CSI AC Electrical Characteristics

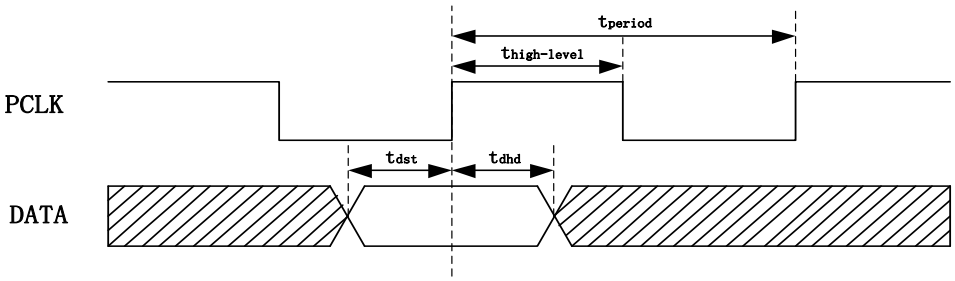


Figure 10-16. Data Sample Timing

Table 10-11. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk Period	t_{period}	5.95	-	-	ns
Pclk Frequency	$1/t_{period}$	-	-	168	MHz
Pclk Duty	$t_{high\text{-}level}/t_{period}$	40	50	60	%
Data input Setup time	t_{dst}	0.6	-	-	ns
Data input Hold time	t_{dhd}	0.6	-	-	ns

10.8.4. CIR Receiver AC Electrical Characteristics

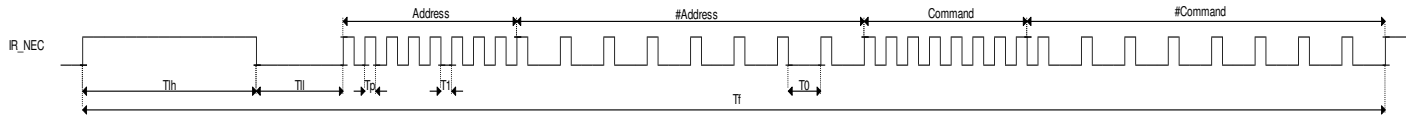


Figure 10-19. CIR Receiver Timing

Table 10-14. CIR Receiver Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Frame Period	Tf	-	67.5	-	ms
Lead Code High Time	Tlh	-	9	-	ms
Lead Code Low Time	Tll	-	4.5	-	ms
Pulse Time	Tp	-	560	-	us
Logical 1 Low Time	T1	-	1680	-	us
Logical 0 Low Time	T0	-	560	-	us

10.8.5. SPI AC Electrical Characteristics

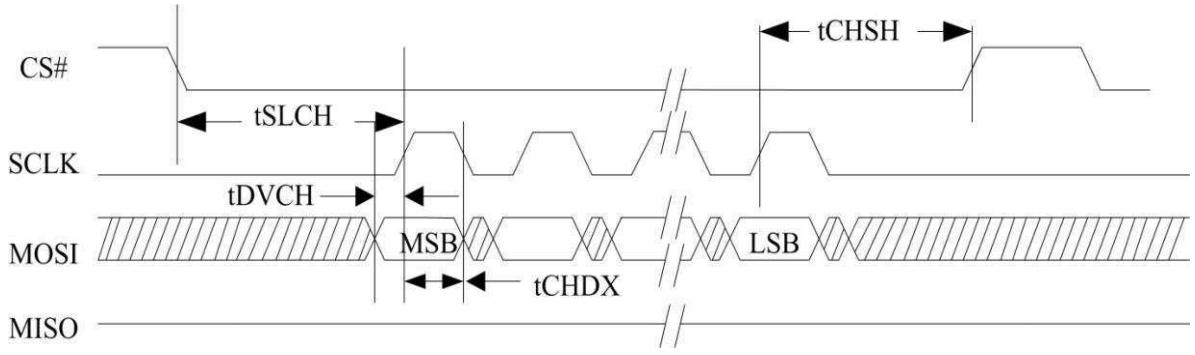


Figure 10-20. SPI MOSI Timing

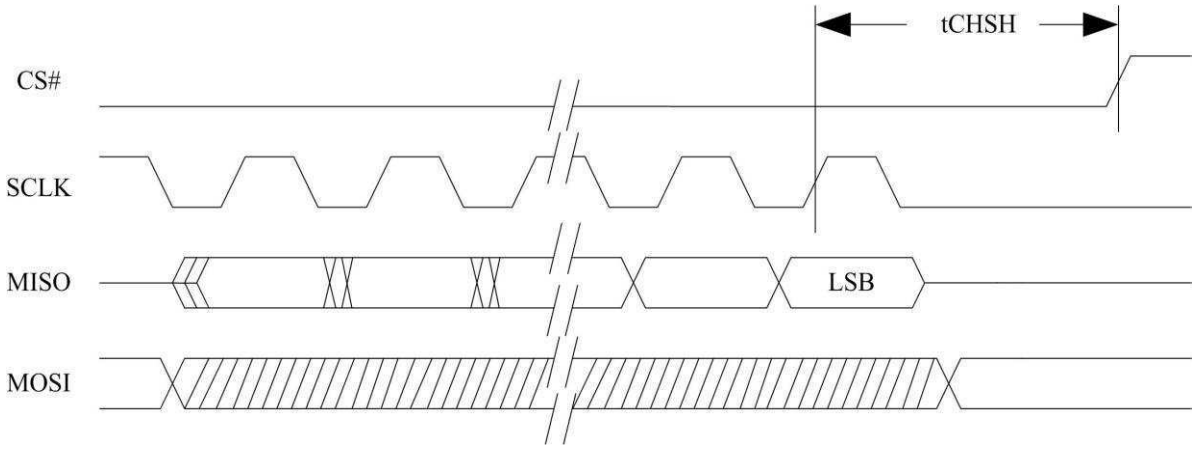


Figure 10-21. SPI MISO Timing

Table 10-15. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	tSLCH	-	2T	-	ns
CS# Active Hold Time	tCHSH	-	2T(1)	-	ns
Data In Setup Time	tDVCH	-	T/2-3	-	ns
Data In Hold Time	tCHDX	-	T/2-3	-	ns
Note (1):T is the cycle of clock.					

10.8.6. UART AC Electrical Characteristics

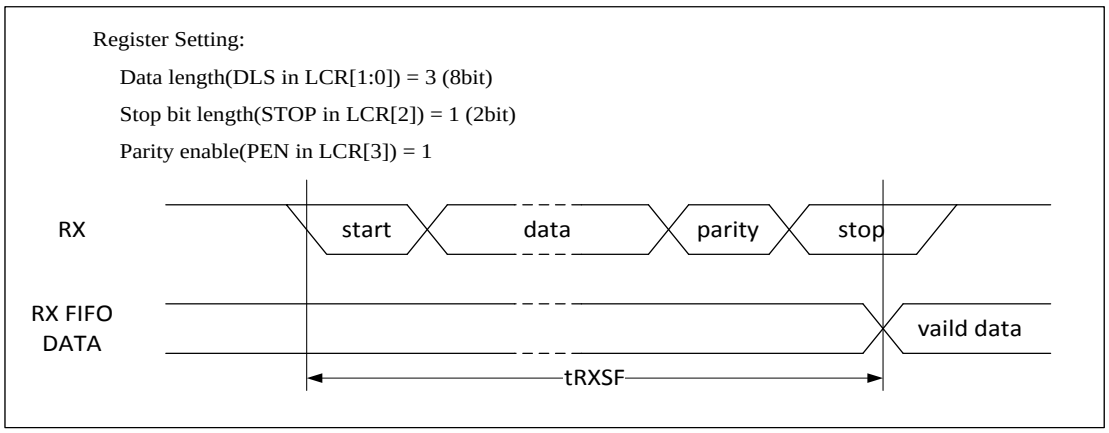


Figure 10-22. UART RX Timing

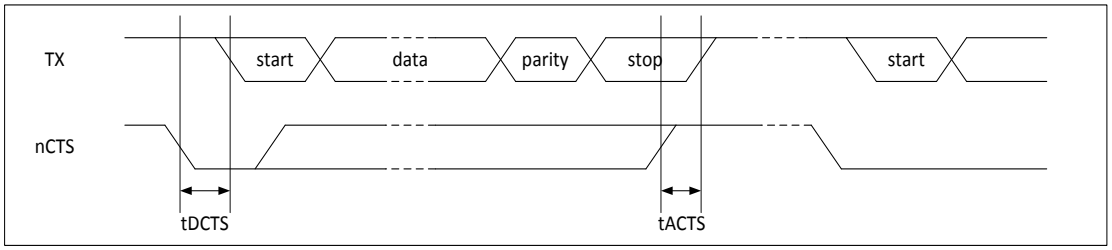


Figure 10-23. UART nCTS Timing

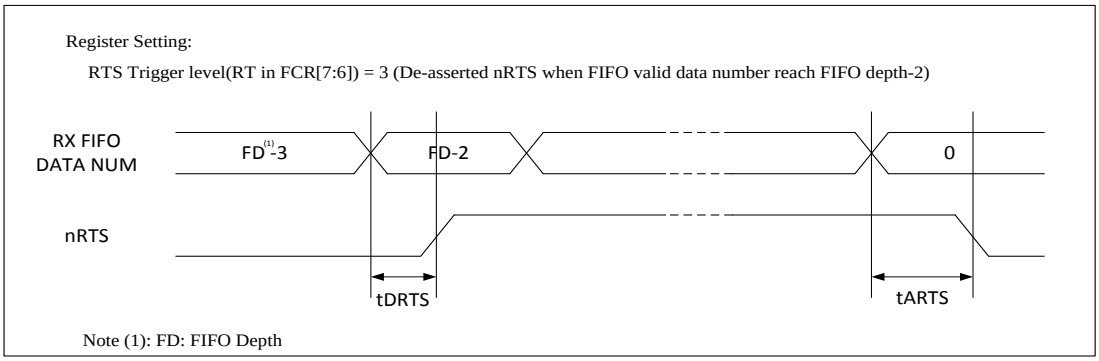


Figure 10-24. UART nRTS Timing

Table 10-16. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
Note (1): BRP(Baud-Rate Period).					

10.8.7. TWI AC Electrical Characteristics

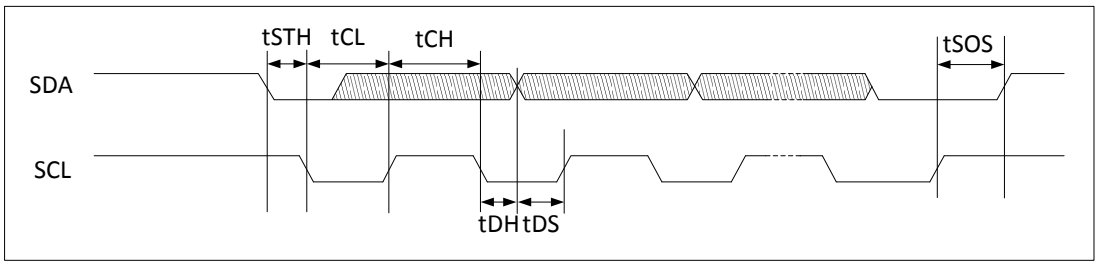


Figure 10-25. TWI Timing

Table 10-17. TWI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
High period of SCL	tCH	0.96	-	-	μs
Low period of SCL	tCL	1.5	-	-	μs
SCL hold time for START condition	tSTH	1.5	-	-	μs
SCL step time for STOP condition	tSOS	1.6	-	-	μs
SDA hold time	tDH	0.82	-	-	μs
SDA step time	tDS	0.72	-	-	μs

10.8.8. TSC AC Electrical Characteristics

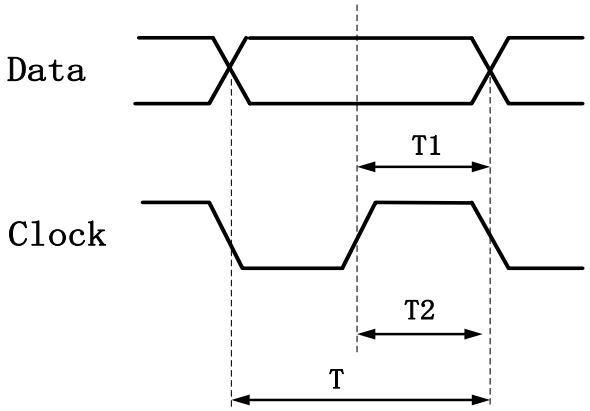


Figure 10-26. TSC Data and Clock Timing

Table 10-18. TSC Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Data hold time	T1	T/2-T/10	$T^{(1)}/2$	T/2+T/10	us
Clock pulse width	T2	T/2-T/10	T/2	T/2+T/10	us
Note (1):T is the cycle of clock.					

10.8.9. SCR AC Electrical Characteristics

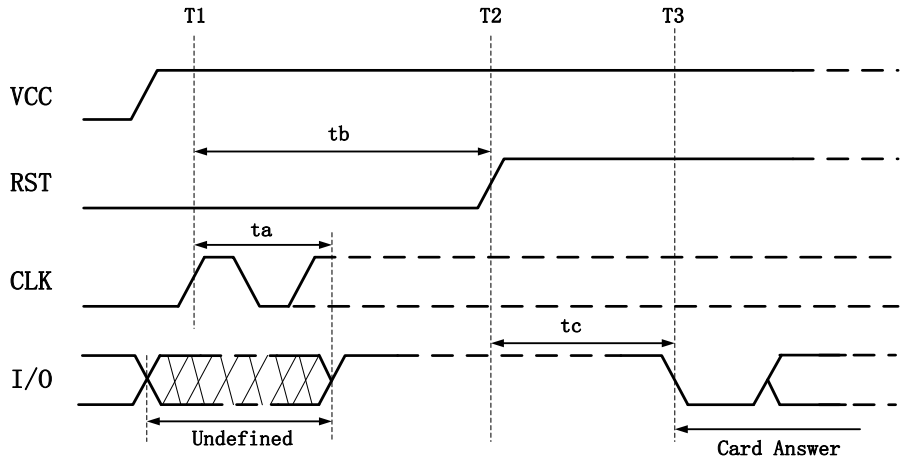


Figure 10-27. SCR Activation and Cold Reset Timing

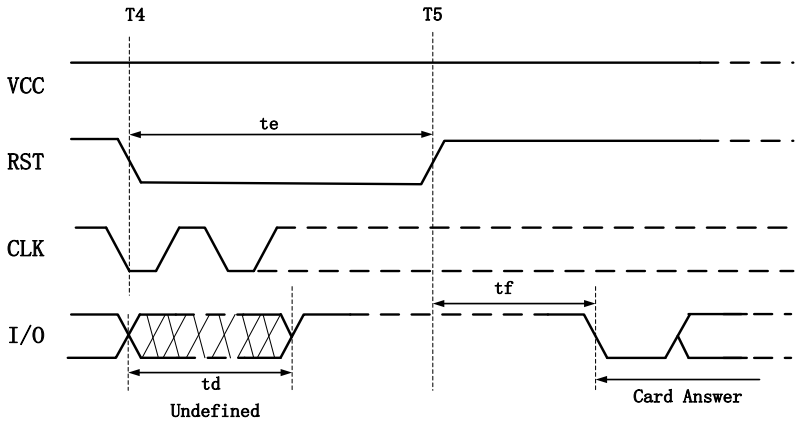


Figure 10-28. SCR Warm Reset Timing

Table 10-19. SCR Timing Constants

Symbol	Min	Type	Max	Unit
ta	-	-	200/f	us
tb	400/f	-	-	us
tc	400/f	-	40000/f	us
td	-	-	200/f	us
te	400/f	-	-	us
tf	400/f	-	40000/f	us

Note:

(1). Activation: Before time T1

(2). Cold Reset: After time T1

(3). T1: The clock signal is applied to CLK at time T1.

(4). T2: The RST is put to state H.

(5). T3: The card begin answer at time T3

(6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
(7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
(8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
(9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
(10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12). f is the frequency of clock.

10.9. Power-up and Power-down Sequence

The following figure shows an example of the power-up sequence for H5 device. During the entire power-up sequence, the RESET pin must be held on low until all power domains are stable. The other power domains not in Figure 10-29 can be turned on upon the software request.

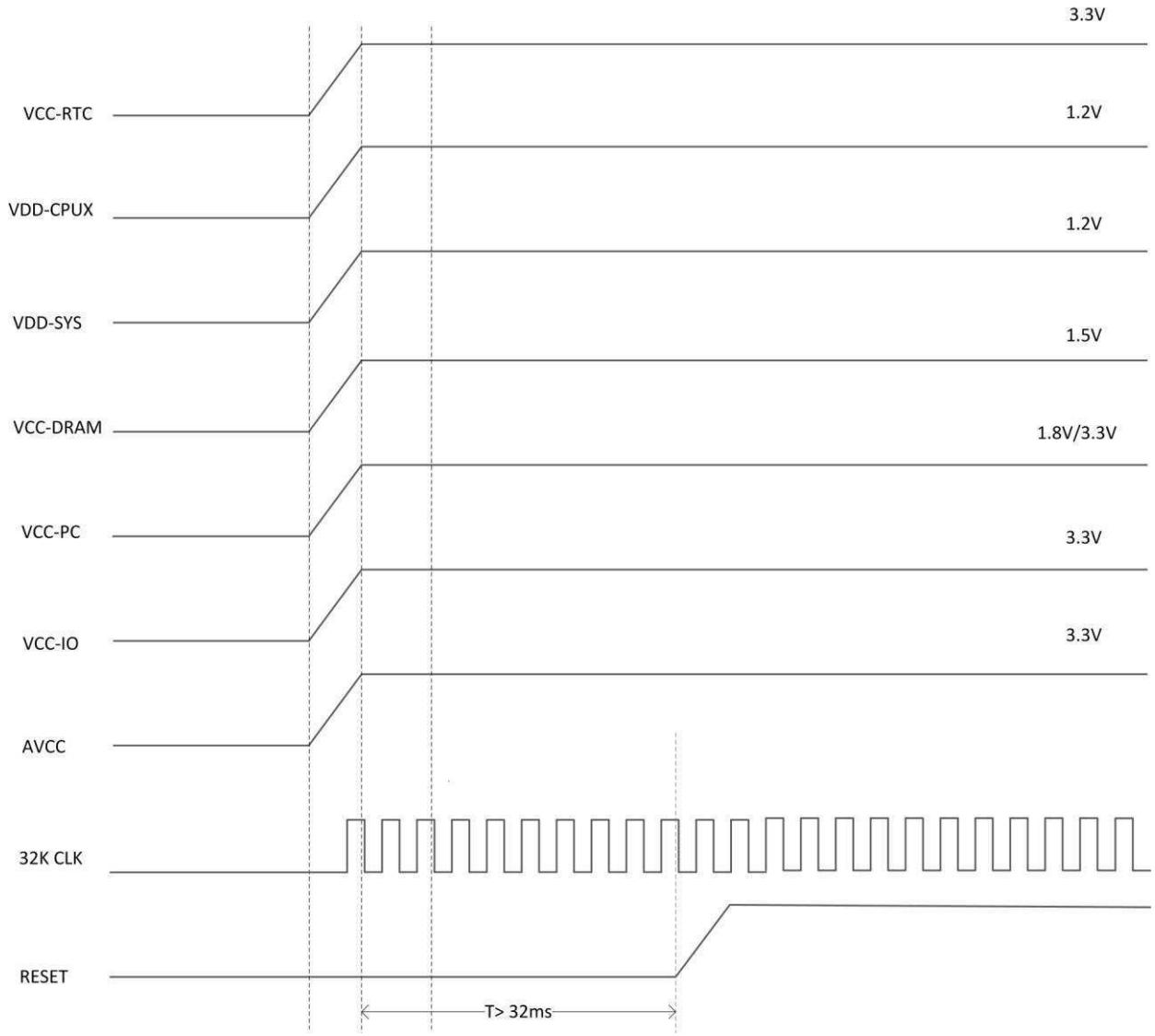


Figure 10-29. Power On Sequence

Power-down sequence is not special restrictions for H5.

10.10. Package Thermal Characteristics

For reliability and operability concerns, the absolute maximum junction temperature of H5 has to be below 125°C.The testing PCB is based on 4 layers. The following thermal resistance characteristics in Table 10-20 is based on JEDEC JESD51 standard, because the system design and temperature could be different with JEDEC JESD51 , the simulating result data is a reference only, please prevail in the actual application condition test.

Table 10-20. H5 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
T_J	Junction Temperature	-	-	+125	°C

θ_{JA}	Junction-to-Ambient Thermal Resistance	-	27.9	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	TBD	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	TBD	-	°C/W
ψ_{JT}	Junction-to-Top Characterization Parameter	-	TBD	-	°C/W
ψ_{JB}	Junction-to-Board Characterization Parameter	-	TBD	-	°C/W

(1). These values are based on a JEDEC-defined 2S2P system and will change based on environment as well as application.

(2). °C/W : degrees Celsius per watt.

Appendix

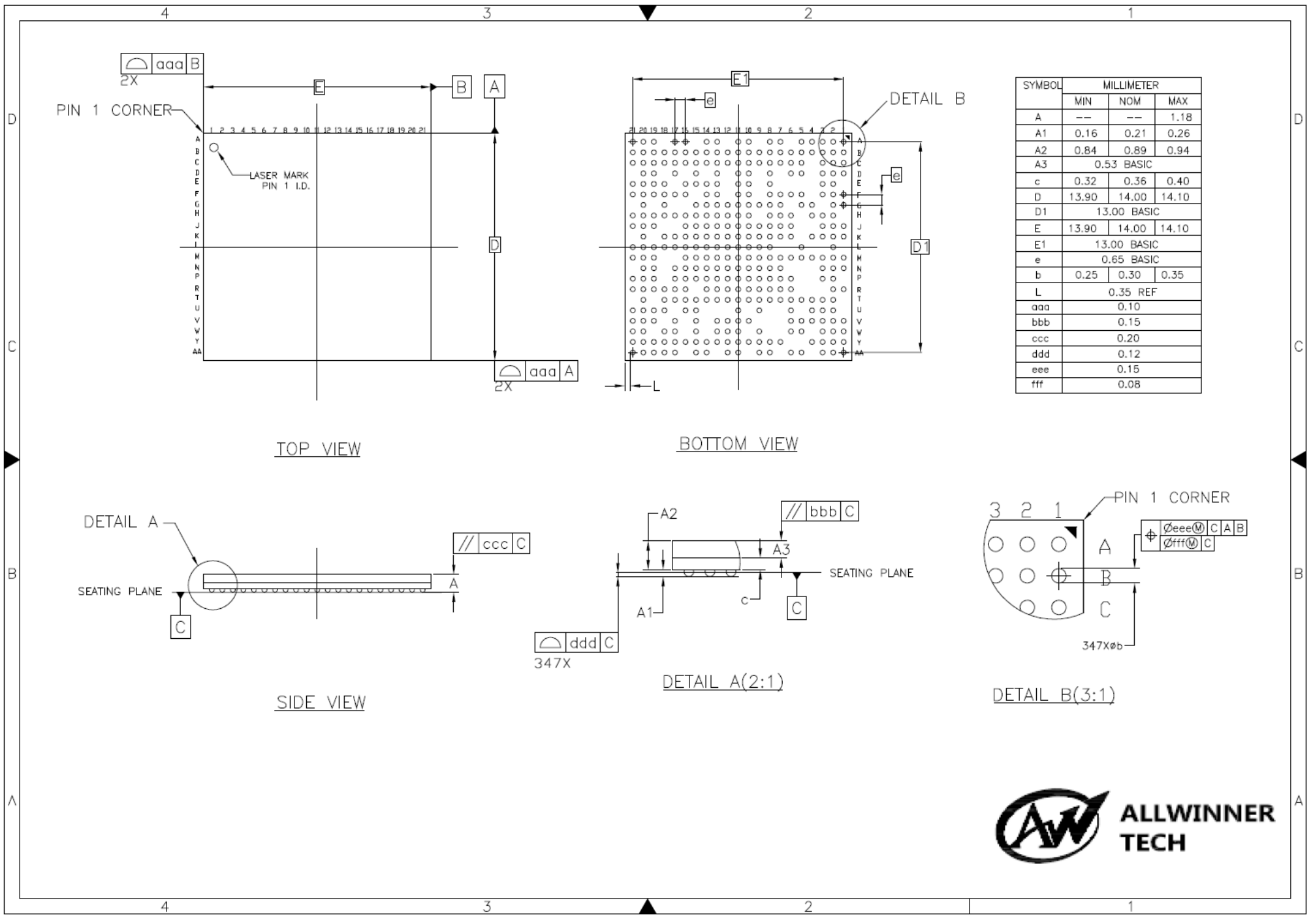
Pin Map

The following figure shows the pin maps of the 347-pin FBGA package of H5 processor.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	JTAG-SEL0	EPHY-LINK-LED	EPHY-TXN	EPHY-RXN	USB-DP0		USB-DP2	USB-DM2		PE1	PE11		PA20	PA21		PC7	PC5		PF1	PD4	GND	A
B	PG13	JTAG-SEL1	EPHY-TXP	EPHY-RXP	USB-DM0	USB-DP1	USB-DM1	USB-DP3	USB-DM3	PE0	PE2	PE12	PA18	PA19	PC3	PC2	PC12	PC8	PC13	PD2	PD6	B
C	PG5	PG4	PG8		PE15	PE14	PE13	PE7	PE4	PE3	PE8	PE9	PA12	PA17	PC0	PC1	PC9	PC11	PC15	PF5	PD0	C
D	PG12	PG11	PG7		PA1	PA2		PA7		PE6	PA0		PA9		PA16		PC10		PF0	PF2		D
E		HTXCN	PG9					PE10		PE5	PA10		PA3	PA6	PA13	PC6		PD7	PD12	PD8	PF4	E
F	HTX0N	HTXCP	PG3		PA4	EPHY-RTX	EPHY-SPD-LED	EPHY-VDD		TVOUT	PA11		PA8	PA15		PC4	PC14	PF3	PD5	PD11	PD9	F
G	HTX0P	HTX1N		PG6	HCEC		EPHY-VCC	GND	V33-TV	VDD-EFUSE	VCC-USB	PA14	VCC-IO	VCC-IO	VCC-PC			PF6		SDQM1		G
H		HTX1P	HSCL	PG2		PA5	VCC-PG	GND		VDD-SYS	VDD-EFUSEBP	GND	VCC-IO	VCC-IO	GND	PC16	PD1	PD3	PD10	SDQ9	SDQ10	H
J	HTX2P	HTX2N	PG0			HVCC	VDD-CPUS	VDD-CPUS	GND	VDD-SYS	VDD-SYS	VDD-GPUFB	GND	VCC-IO	VCC-PD	GND			SDQ8	SDQS1B	SDQ11	J
K	X24MOUT	X24MIN	HSDA	X24MFOUT		VCC-RTC	GND	GND	GND	VDD-SYS	VDD-SYS	VDD-SYS	GND	GND	GND	GND	PD13	PD15		SDQS1		K
L		PG1			PLLTEST			GND	GND	VDD-SYS	VDD-SYS	VDD-SYS	VDD-SYS	VDD-SYS	GND	VCC-DRAM	PD14	PD16	PD17	SDQ12	SDQ13	L
M	PL1	HHPD	PG10	RTC-VIO	GND	PL9	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC-DRAM			SDQ15	SDQM0	SDQ14	M
N	PL0	PL4	VCC-PLL				GND	VDD-CPUX	GND	GND	GND	GND	GND	GND	GND	VCC-DRAM	SA14		SA11	SDQ0		N
P		PL2	X32KFOUT			VDD-CPUX	VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	GND	GND	GND	GND	GND	VCC-DRAM	VCC-DRAM		SA10	SDQ2	SDQ1	P
R	PL3	PL5				VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	GND	GND	GND	GND	GND		VCC-DRAM	SA15	SA12	SDQ4	SDQS0	SDQS0B	R
T		PL8	PL7	PL6	TEST	VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	VDD-CPUFB	GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	SVREF	SA0	SBA1		SDQ5		T
U		PL11	AGND	X32KOUT		VDD-CPUX			VDD-CPUX		VCC-DRAM				SCAS	SRST		SA1	SDQ6	SDQ7	SDQ3	U
V	LINEINL	PL10	AVCC	VRP	X32KIN	RESET				SZQ	SODT1	SA13	SRAS		SA7		SBA2		SA2	SA3	SA4	V
W	LINEINR	MICIN1P	MBIAS		VRA2	UBOOT			SDQ28		SODT0	SDQ24	SWE		SDQ19		SBA0	SA8		SCS0	SCS1	W
Y	MICIN1N	MICIN2P	LINEOUTR	VRA1			SDQ31	SDQ30	SDQS3B	SDQ27	SDQ26	SDQ23	SDQ22	SDQ20	SDQS2B	SDQ18	SDQ16	SA9	SA5	SA6	SCKE1	Y
AA	GND	MICIN2N	LINEOUTL		KEYADC	NMI		SDQ29	SDQS3		SDQ25	SDQM3		SDQ21	SDQS2		SDQ17	SDQM2	SCK	SCKB	SCKE0	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Package Dimension

The following diagram shows the package dimension of H5 processor, includes the top, bottom, side views and details of the 14mmx14mm package.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.18
A1	0.16	0.21	0.26
A2	0.84	0.89	0.94
A3	0.53 BASIC		
c	0.32	0.36	0.40
D	13.90	14.00	14.10
D1	13.00 BASIC		
E	13.90	14.00	14.10
E1	13.00 BASIC		
e	0.65 BASIC		
b	0.25	0.30	0.35
L	0.35 REF		
aaa	0.10		
bbb	0.15		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		