Embedded Systems Week
www.esweek.org
October 10-15, 2021
Virtual Conference

CODES+ISSS 2021

Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis
October 10 – October 15, 2021, *Virtual Conference*

The International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) is the premier conference in system-level design, hardware/software co-design, modeling, analysis, and implementation of modern Embedded Systems, Cyber-Physical Systems, and Internet-of-Things, from system-level specification and optimization to system synthesis of multi-processor hardware/software implementations. CODES+ISSS is part of Embedded Systems Week (ESWEEK), the premier event covering all aspects of hardware and software design for smart, intelligent and connected computing systems.

Journal Track Submissions:
Abstracts: April 2, 2021
Full Papers: April 9, 2021 (firm)
Work-in-Progress Submissions:
Full Papers: June 4, 2021 (firm)
Notification of Acceptance:
July 5, 2021 (both tracks)

CODES+ISSS Program Chairs:
Jason Xue, City University of Hong Kong, China
Chengmo Yang, University of Delaware, USA

Topics of interest include:

Track 1) System-level design – Specification, modelling, refinement, synthesis, and partitioning of embedded systems, hardware-software co-design, design space exploration, hybrid system modeling and design, model-based design, design for adaptivity and reconfigurability.

Track 2) Domain and application-specific design – Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, IoT, neural network, and other application domains.

Track 3) Embedded software – Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, middleware.

Track 4) System architecture – Heterogeneous systems, many-cores, networked and distributed systems, architecture and micro-architecture design, exploration and optimization including application-specific processors and accelerators, reconfigurable and self-adaptive architectures, storage, memory systems, and networks-on-chip.

Track 5) Simulation, validation and verification – Hardware/software co-simulation, verification and validation methodologies, formal verification, hardware accelerated simulation, simulation and verification languages, models, and benchmarks.

Track 6) Safety, security and reliability – Cross-layer reliability, resilience and fault tolerance, test methodology, design for security, reliability, and testability, hardware security, security for embedded, CPS, and IoT devices.

Track 7) Power-aware systems – Power-aware and energy-aware system design and methodologies, ranging from low-power embedded and cyber-physical systems, IoT devices, to energy-efficient large-scale systems such as cloud datacenters, green computing, and smart grids.

Track 8) Embedded machine learning – Hardware and software design, implementation, and optimization for machine learning that are specially designed for resource- and power-constrained embedded, CPS, and IoT devices.

Track 9) Industrial practices and case studies – Practical impact on current and/or future industries, application of state-of-the-art methodologies and tools in various application areas including wireless, networking, multimedia, automotive, cyber-physical, medical systems, IoT, etc.

Journal-Integrated Publication Model: CODES+ISSS 2021 has a dual publication model with two tracks. Journal track papers will be published in the ACM Transactions on Embedded Computing Systems (TECS) and Work-in-Progress track papers will be published in the ESWEEK Proceedings. See details at http://www.esweek.org/author-information

ESWEEK General Chairs:
Andreas Gerstlauer, University of Texas at Austin, USA
Aviral Shrivastava, Arizona State University, USA

CODES+ISSS Program Chairs:
Jason Xue, City University of Hong Kong, China
Chengmo Yang, University of Delaware, USA